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Application Guide:

Exar Product Handling & Reliability

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Note: This application guide is intended for general reference and may be subject to change. Contact Exar Sales or QA for critical or special application requirements.

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GENERAL INFORMATION ABOUT EXAR

1.0 EXAR

Exar Corporation designs, develops and markets innovative, system oriented mixed-signal integrated circuits for high-speed broadband communication and data acquisition markets. The company, based in Fremont, California, employs approximately 265 people worldwide. Please refer to Exar's web page, www.exar.com, for further information.

1.1 MANUFACTURING

Wafer Processing, Packaging, and Assembly:
Exar is a fabless, assemblyless company that works with selected qualified silicon foundries and assembly subcontractors to determine optimum and economical wafer processing technology and packages for products designed by Exar. Exar mainly follows EIA/JEDEC standards and applicable industry standards for package configuration, process monitor, and reliability tests.

Electrical Testing:
Wafer-level and/or package-level electrical testing is designed to ensure products meet or exceed the design product specification and customers' requirements. All standard products are subjected to 100% electrical testing in addition to QA sample testing at room temperature prior to shipment to customers. Products are tested either in-house or by an approved subcontractor.

1.2 ODS (Ozone Depleting Substance) Policy:

Exar and its suppliers have adopted and complied with an ODS-free policy for all products and related manufacturing processes.

1.3 Pb-Free / RoHS Solutions:

Environmental Policy:

Exar Corporation is committed to protecting the environment and individual health and safety. We shall comply with all environmental regulations, health and safety laws applicable to our business. We employ continual efforts to minimize the environmental impact of our products.

Environmental Highlights:

1. All Exar products are free from mercury, cadmium, hexavalent chromium, PBB, and PBDE and they are in compliance with European RoHS requirements except for lead. Lead-free products are also available upon request.

2. Current qualified Pb-free lead finish for hermetic CDIP is hot-dipped Sn/0.7%Cu. hot-dipped SAC (SnAgCu) is under engineering evaluation and qualification.

3. Exar has qualified and implemented green mold compounds to replace those compound that contain brominated flame retardant.

4. Pb-free alternative, Sn/Ag/Cu (SAC) for ball array packages such as PBGA has been evaluated and qualified by Exar's assembly suppliers. The available solder ball composition is Sn/3%Ag/0.5%Cu (nominal).

5. Exar is using matte tin for the lead finish for lead-free lead-frame products. A post-plating heat treatment at 150C/1hr is applied to mitigate tin whisker growth in the field.

6. Exar will continue to support both non-lead-free and lead-free products after 7/1/2006 until notified otherwise.

7. Exar lead-free products are compatible with standard Sn/Pb board assembly. Moisture-sensitive parts are dry packed and customers need to pay attention to the bag labels for handling instructions.

8. Exar key assembly suppliers and foundries are certified to ISO 14001, Environmental Management System Requirements.

1.4 Pb-Free Identification:

To identify a Pb-free part, Exar has adopted and implemented the following policy for Pb-free tracking purpose.

a. Pb-free part numbers shall carry "-F" suffix unless otherwise specified, e.g. XRT73L03IV-F. The "–F" P/N is required when placing orders for Pb-free version of Exar standard parts. The Pb-free suffix will be shown on all device and packing labels. In addition, a Pb-free symbol will be shown on MSL-1 and moisture warning labels (see diagrams next).

b. Pb-free identifier, "F", shall be marked (both top and bottom if applicable) on Pb-free packages as prefix to datecode (YYWW) unless otherwise specified (e.g. F suffix to YYWW for QFN's).

c. Pb-free lead finish or solder ball composition is also listed on MSL-1 and moisture warning labels as e1, e2, or e3 where e1=Sn/Ag/Cu, e2=Sn/Cu, and e3=matte Sn.

Pb
RoHS

ex

LEVEL
1

NOT MOISTURE SENSITIVE

These devices do not require special storage conditions provided:

1. They are maintained at conditions equal to or less than 30°C/85% RH, and

2. They are solder reflowed at a peak body temperature which does not exceed 250°C.

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Pb
RoHS

ex

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
2a
If blank, see adjacent bar code label

1. Calculated shelf life sealed bag: 12 months at <40°C and <90% relative humidity (RH)
2. Peak package body temperature: _____°C
   If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: _____ hours of factory conditions
   If blank, see adjacent bar code label
   <30°C/60% RH, OR
   b) Stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is >10% when read at 23+/-5°C
   b) 3a or 3b not met
5. If baking is required, devices may be baked for 48 hours at 125+/-5°C
   Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: _____
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Note: ex

e1 Sn/Ag/Cu 2nd level interconnect
e2 Sn/Cu 2nd level interconnect
e3 matte Sn 2nd level interconnect

1.5 Known Hazardous/Regulated Substances:

To Exar's best knowledge, Exar products in plastic IC packages contain the following known hazardous or regulated substances as listed below. In an additional effort to move towards more "green" (environmental friendly) packaging, Exar has qualified new packaging materials such as "green" mold compounds that contain no flame retardant and exhibit better reliability especially for Pb-free soldering condition.

List of Substances with Environmental Impact						
Type	**Substance**	**O Yes**	**X No**	**Content % wt**	**Use**	**Remark**
Metal and Its Compound / Inorganic	Antimony and its compounds	**O**		100-300ppm	Flame retardant in mold compounds, substrate	PDIP/SO/SSOP/PLCC/ QFP/QFN/PBGA
	Arsenic and its compounds		**X**			
	Beryllium and its compounds		**X**			
	Cadmium and its compounds		**X**			
	Hexavalent chromium and its compounds		**X**			
	Cobalt and its compounds		**X**			
	Lead and its compounds	**O**		2000-4000ppm	Solder lead finish or solder ball	Pb-free option is available
	Mercury and its compounds		**X**			
	Selenium and its compounds		**X**			
	Tellurium and its compounds		**X**			
	Thallium and its compounds		**X**			
	Barium		**X**			
	Silver	**O**		3000-7000ppm	Spot plating on lead frame bond fingers and die attach pad, fillers for die attach material	Plastic packages
	Metal carbonate		**X**			
	Asbestos		**X**			
	Cyanide		**X**			
	Nickel and its compounds	**O**		10000-30000ppm	Lead frame material alloy	CDIP and QFP/LQFP/TQFP
	Iron and its compounds	**O**		2000-8000ppm	CDIP lead frame material alloy	CDIP only
	Manganese and its compounds	**O**		50-150ppm	Lead frame material alloy	QFP/LQFP/TQFP only
	Copper and its compounds	**O**		300000-900000ppm	Lead frame base material	Plastic leaded/leadless pkgs
	Aluminum and its compounds	**O**		100-200ppm	Bonding wires, interconnect metal on semiconductor Ics, CDIP frame bond area	Al wire for ceramic DIP only, Al interconnect for all Si devices
	Gold and its compounds	**O**		500-1000ppm	Bonding wires	All plastic packages

List of Substances with Environmental Impact						
Type	**Substance**	**O Yes**	**X No**	**Content % wt**	**Use**	**Remark**
Brominated / Chlorinated Organic Compound	Polychlorinated Biphenyls (PCB)		X			
	Polychlorinated Naphthalenes (PCN)		X			
	Chlorinated Paraffins (CP)		X			
	Mirex (Perchlordecone)		X			
	Polybromobiphenyleters (PBBE)		X			
	Triphenyl Polychloride		X			
	Bis(2-Chloroethyl) Ether		X			
	Bis(Chloromethyl) Ether		X			
	Benzotrichloride		X			
	Polychlorinated naphthalene		X			
	PVC and PVC blends	O		100%	Shipping tubes, reel material (all pkgs)	DIP/SO/SSOP/TSSOP/PLCC
	Vinyl Chloride (monomer)		X			
	Polybrominated Biphenyls (PBB)		X			
	Polybrominated Diphenylethers (PBDE)		X			
	Tetrabromobisphenol-A-bis-(2,3-Dibromopropylether) (TBBP-A-bis)		X			
	1.1.1-trichloroethane		X			
	Carbon Tetrachloride		X			
	Methyl Bromide		X			
	Trichloroethylene		X			
	Tetrachloroethylene		X			
	Methylene Chloride		X			
	Brominated Organocompound	O		200-600ppm	Flame retardant in mold compounds, substrates	PDIP/SO/SSOP/PLCC/ QFP/QFN/BGA
Other Organic Substances	Phenol (monomer)		X			
	Organic Tin compounds (tributyl tin compound, triphenyl tin compound)		X			
	Alkyl mercury compounds		X			
	Organic phosphorus compounds		X			
	Polycyclic aromatic hydrocarbon (monomer)		X			
	CFC, HCFC, HBFC		X			
	Halons		X			
	(NUN)-dimethylacetaminde (DMA) and (N)-methylacetaminde (MA)		X			
	Diethylamine and dimethylamine		X			
	Nitrosaminde and nitrosamine		X			
	Ethylene glcol ethers and their acetates		X			
	Phtalates		X			
	Formaldehyde		X			
	Hydrazine		X			
	Picric acid		X			
	Halogenated aromatic hydrocarbons		X			
	Ploychlaratriphenyls (PCT)		X			
	Pentachlorphenol (PCP)		X			
	Diozines		X			
	Halogemated dibenzofurances		X			
	Ethylene oxide		X			
	1,2-Dichloroethane		X			
	1,1-Dichloroethylene		X			
	Carbon tetrachloride		X			
	Azo compounds		X			
	Polyvinyl Chloride (PVC) and PVC blends		X			
	Fluorine and its compounds		X			

List of Substances with Environmental Impact						
Type	**Substance**	**O Yes**	**X No**	**Content % wt**	**Use**	**Remark**
Other Organic Substances	Toluence		X			
	Xylene		X			
	Ester Phthalate		X			
	Epichlorohydrin		X			
	Acrylonitrile		X			
	Salts of O-tolidine		X			
	Threosulfan		X			
	Salts of 4-nitrobiphenyl		X			
	Salts of Benzene		X			
	Erionite		X			
	Salts of 4-aminodiphenyl		X			
Others	Radioactive Substances		X			
	DDT		X			
	Dieldrin		X			
	Endrin		X			
	Chlordane		X			

Note:

1. This list is based upon Exar's best knowledge at the time of publication. Any update or change will be reflected in the next revision.

2. The actual concentration varies with package types and devices. The reported values in this list are for general reference only. More detailed data shall be reported on device basis.

3. Exar is committed to a continual improvement program to address various environmental concerns from the use of potentially hazardous materials in packaging and packing Exar IC products. Examples of the programs are Pb-free lead finish or solder ball, "green" (environmental-friendly) packaging materials, and green or recyclable packing materials. Please contact Exar sales representative for more details.

4. Related Law, Regulation, and Agreement:
   - Montreal Protocol (concerning the protection of ozone layer)
   - Water Pollution Control Law
   - EU RoHS Directive (Restriction of the use of certain hazardous substances)
   - EU Battery Directive
   - EU Directive on Packaging and Packaging Waste
   - WEEE Directive (waste from electrical and electronic equipment)
   - Japan: Law Concerning the examination and regulation of manufacture of chemical substances
   - Japan: Industrial Safety and Health
   - Germany: Regulations on Formaldehyde, Laws for Foods and Consumer Products
   - New York and 16 other US states: Regulations on Heavy Metals in Packaging Materials
   - US OSHA regulations and laws on waste management and environmental protection
   - China RoHS directive and regulations.

1.6 SUPPLIER PARTNERSHIPS

1. Exar has developed a comprehensive supplier partnerships program to monitor and collaborate with selected wafer foundries, assembly/packaging houses, test houses, and other service providers.

2. Suppliers' performance is reviewed with each key supplier on a quarterly basis.

3. A Corrective Action Request (CAR) mechanism provides feedback to suppliers for continual improvement and problem correction.

1.7 QUALITY ASSURANCE

1. Exar adopted TQM (Total Quality Management) for its internal and external supplier quality management philosophy. Our Quality System has been ISO 9001 registered since 1994. Currently, Exar is ISO 9001:2000 certified.

2. While maintaining an active supplier management and monitoring program for suppliers, Exar practices continual quality improvement internally and in the interests of its customers through various cross-functional teams, including the QIT (Executive Quality Improvement Team), Supplier Partnerships Team, MRB (Material Review Board), and QRB (Qualification Review Board).

3. The MRB reviews and makes disposition on discrepant materials, while the QRB tracks all design, material, process, and supplier changes that may affect product reliability or performance in customers' applications. Customers are notified of major changes as defined in Exar's QRB specification.

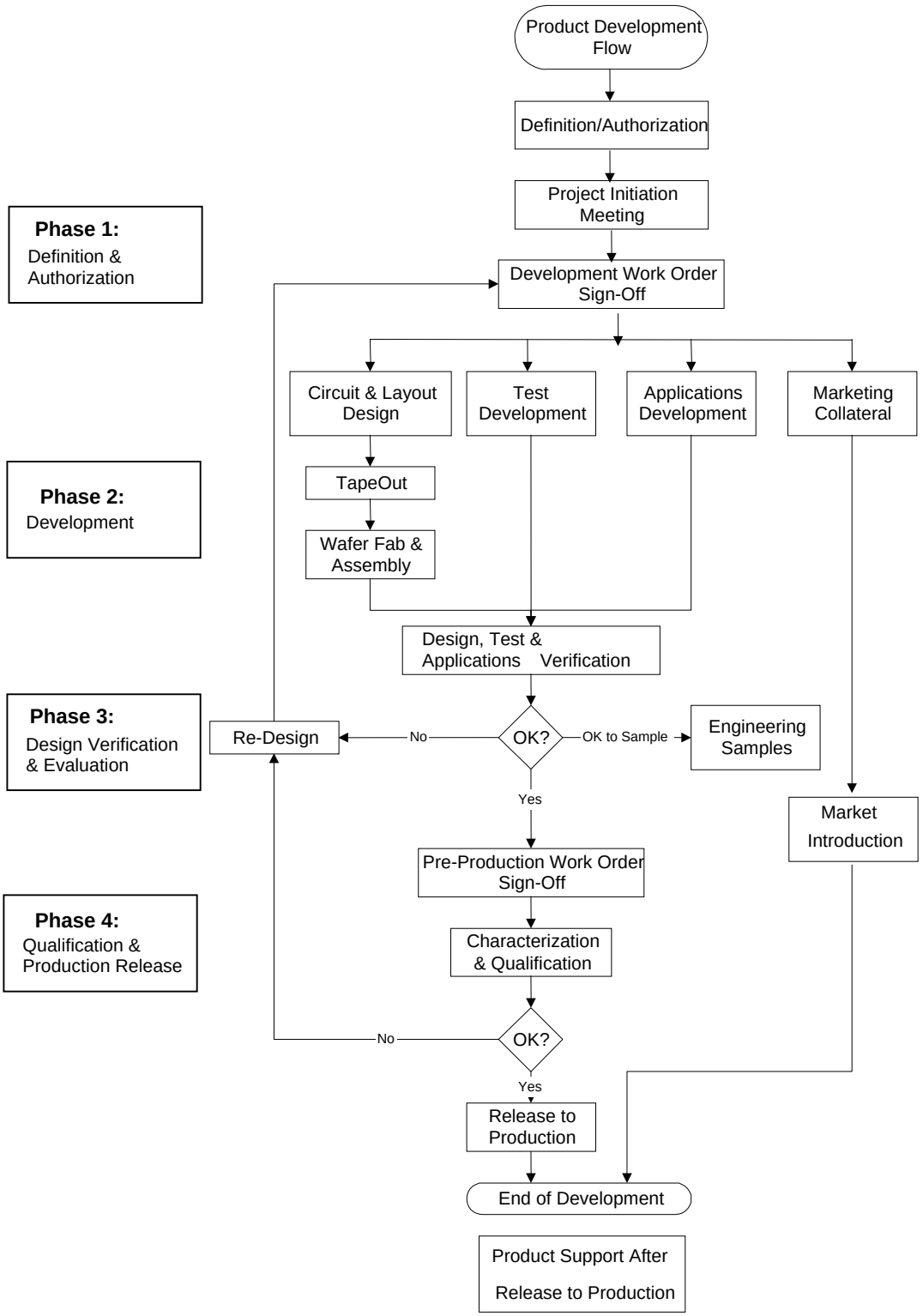
4. The following reference materials are available to provide further details: **Quality Manual**, **Supplier Partnerships Manual**, and **Quarterly Quality and Reliability Report**. Please contact your sales representative for further information.

1.8 FIELD FAILURE AND CLAIM - RMA

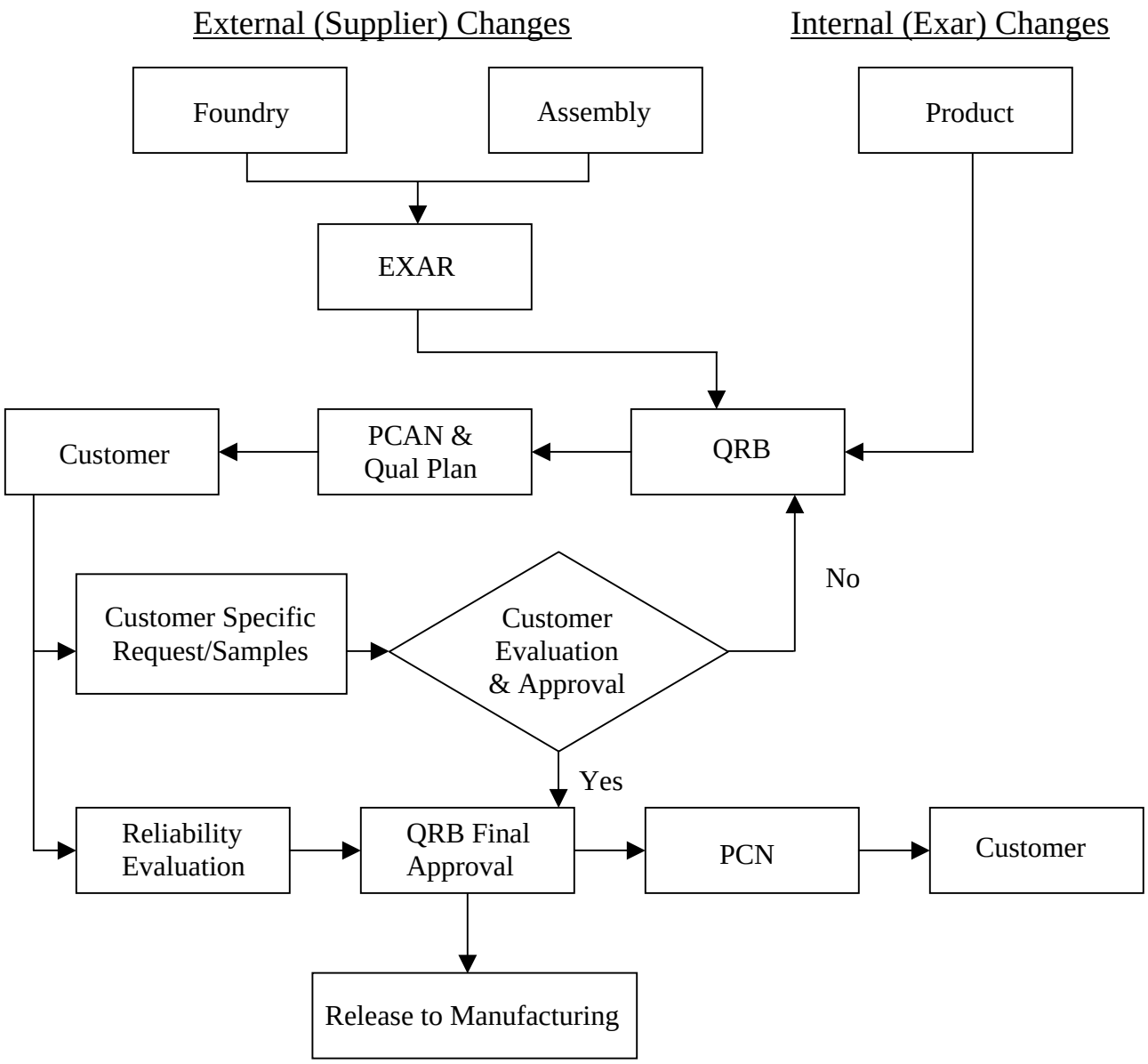
1. In the event of a failure, the customer should contact Exar's sales representative or distributor for an RMA number. If the reason for RMA is due to electrical, mechanical or the reliability of the product, a sample of failures will be requested from the customer for failure analysis prior to issuance of an RMA.

2. To facilitate Exar's investigation, please provide as much information as possible, including a detailed description of the failure or discrepancy, part history after receiving, etc.

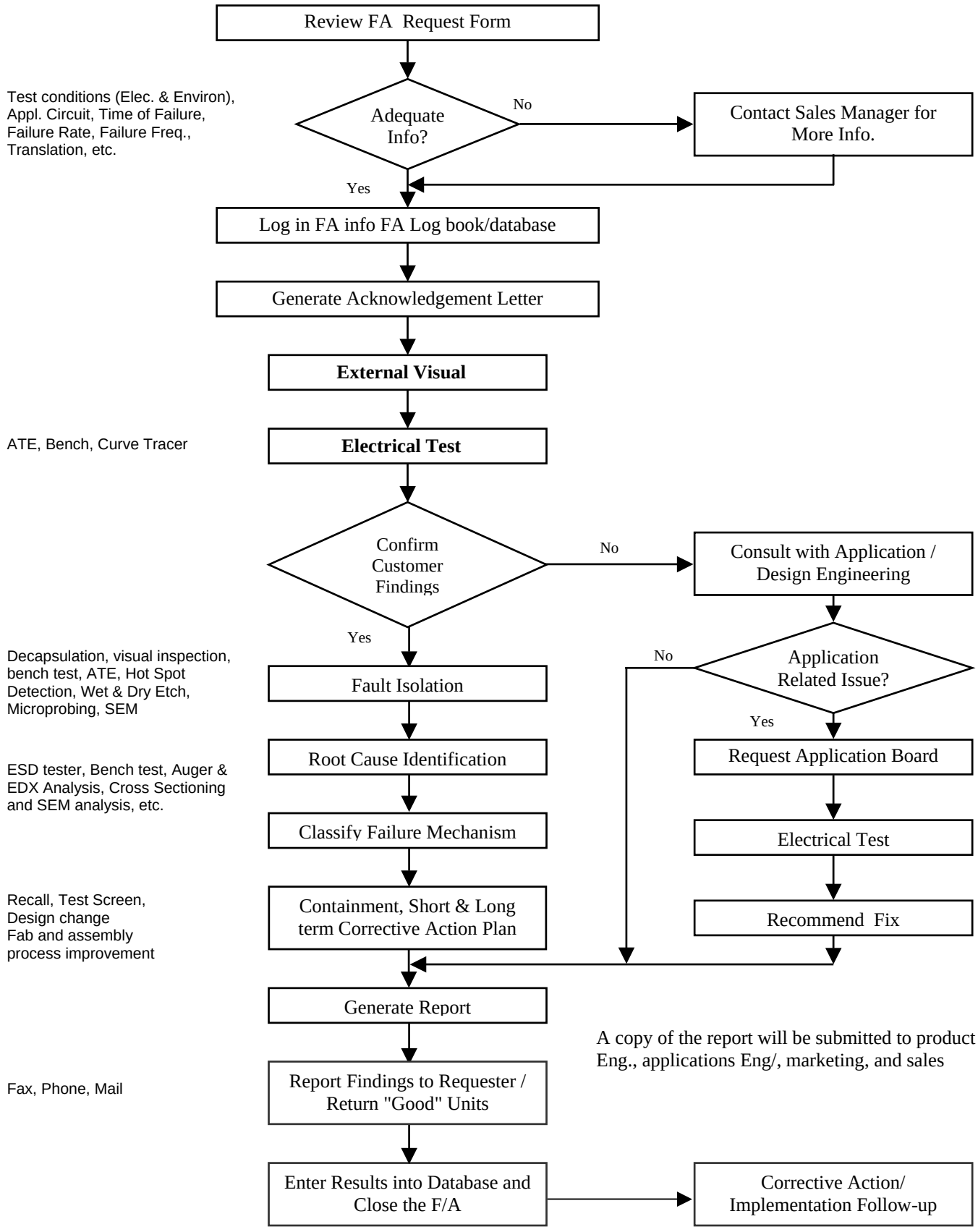
1.9 DESIGN FLOW CHART



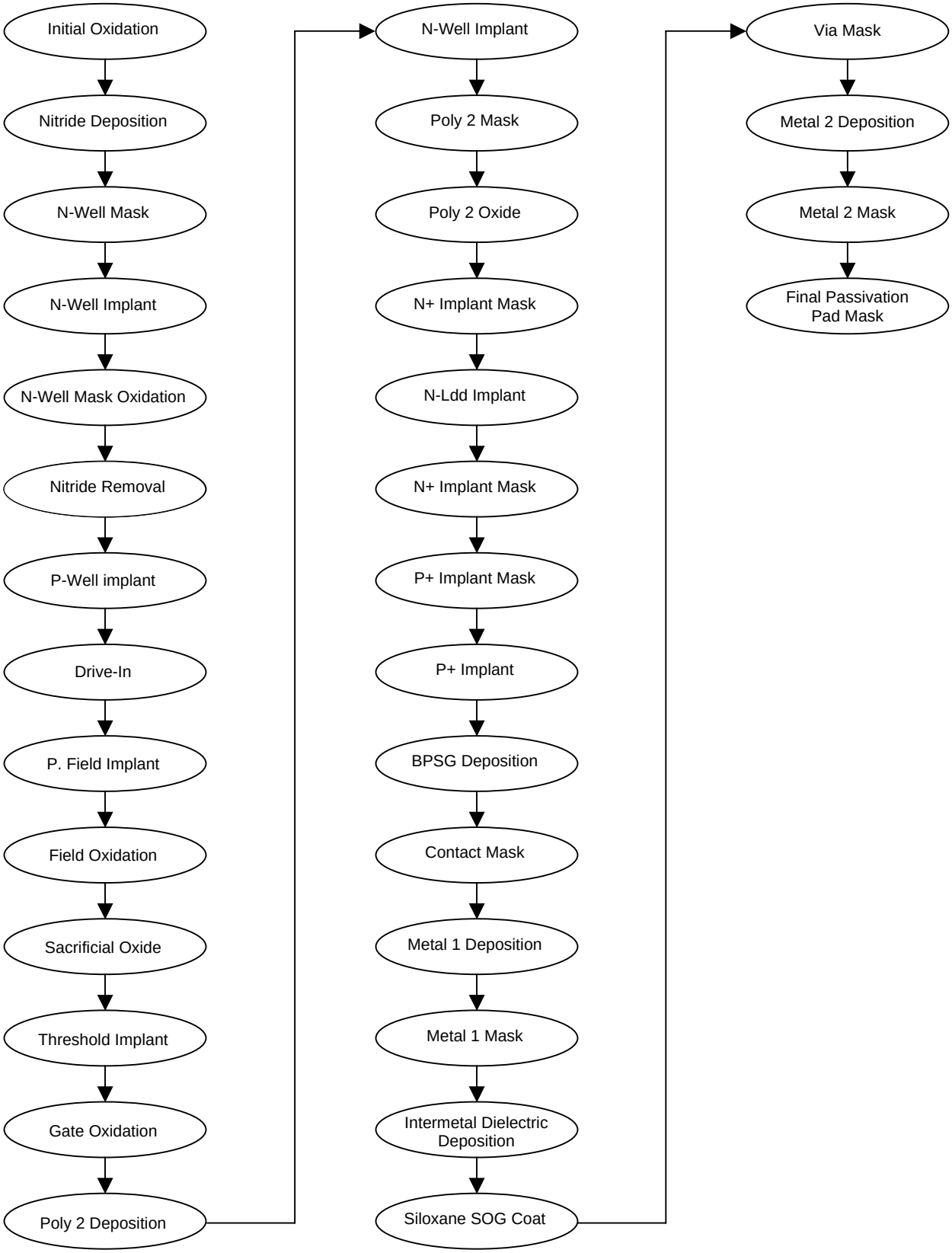
1.10 PROCESS CHANGE NOTIFICATION FLOW CHART – GENERAL GUIDELINES



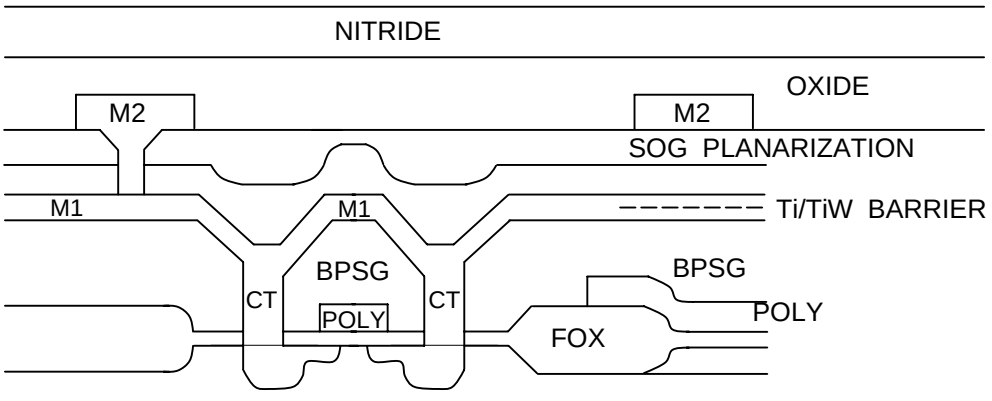
1.11 FAILURE ANALYSIS FLOW CHART



GENERIC WAFER FABRICATION FLOW



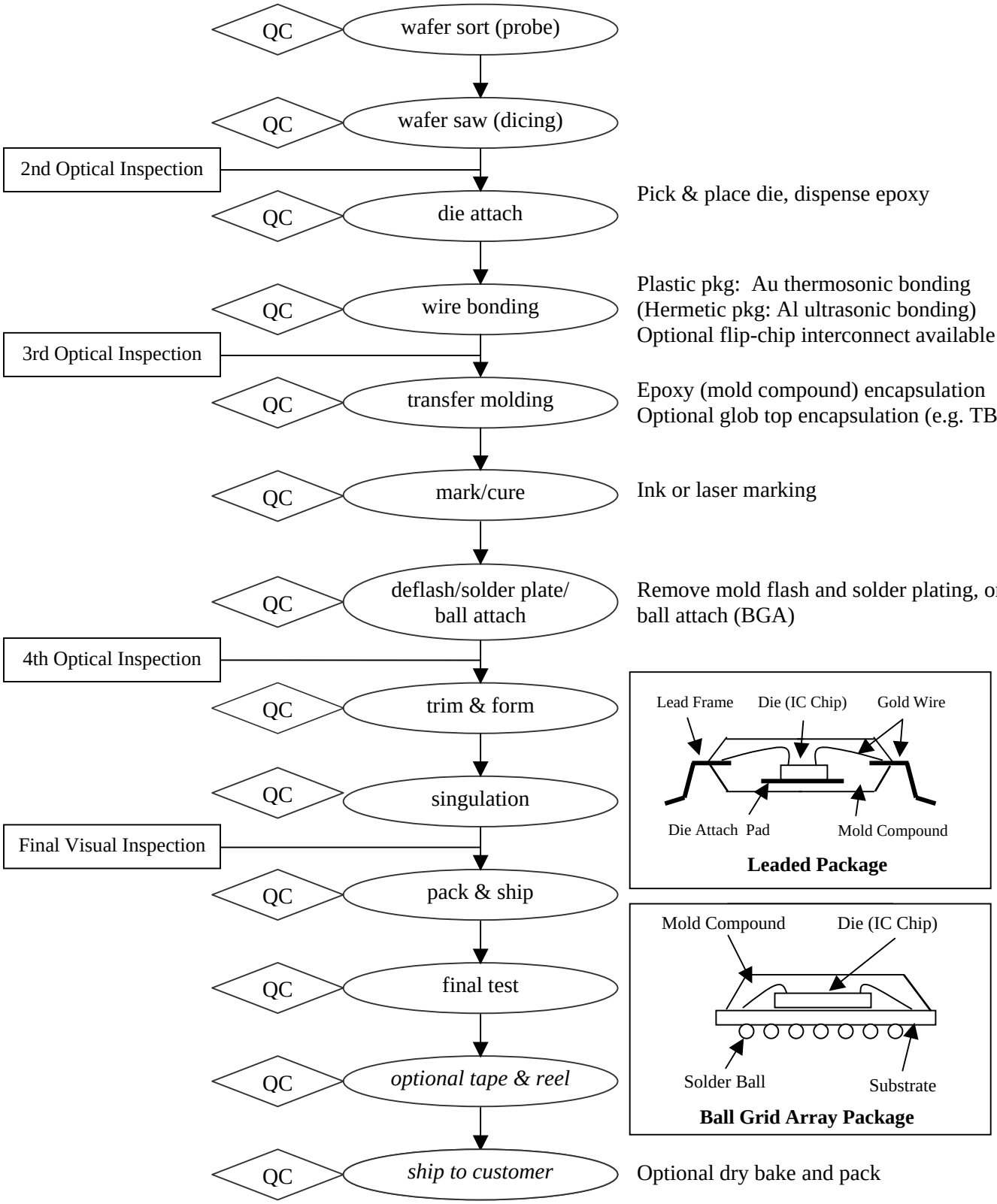
3.0 TYPICAL SILICON CROSS SECTION



Typical CMOS Cross-Section

4.0 GENERIC PLASTIC ASSEMBLY & TEST FLOW

4.1 QC Inspection **4.2 Die attach, wire bond, and molding methods**



5.0 PCB ASSEMBLY GUIDELINES

5.1 SOLDER REFLOW

PCB (printed circuit board) assembly involves attaching ICs and other components to PCB's by applying heat or thermal energy to the joints between component's terminals and PCB's contact pads. Solder material is introduced to the joints through solder dipping, wave soldering, or solder paste printing. A phenomenon of "solder reflow" is achieved when an appropriate amount of heat or thermal energy is applied to the solder joints and raises the temperature of the solder joint above the solder's eutectic point, the lowest temperature where the solder alloy starts to melt. Upon completion of the solder reflow and cool-down in a controlled manner, a satisfactory solder joint is formed with reasonable mechanical strength, metallurgical structure, and electrical conductivity.

5.2 CLEANING & FLUXING

To ensure good quality on PCB assembly, solder joints need to be cleaned thoroughly, normally by using flux to remove oxides and protect the cleaned surface during solder reflow. Flux residuals are then removed with water or solvents, except for those no-clean fluxes that usually leave behind harmless residuals. Although ultrasonic cleaning is not recommended due to the potential damage to delicate IC components, some PCB manufacturers use ultrasound to facilitate the cleaning process. Precautions should be taken to validate and qualify the ultrasonic cleaning process. Water soluble or no-clean fluxes are increasingly popular due to their ease of use.

5.3 REFLOW PROFILE & CONTROLLED HEATING

The common solder reflow methods for SMD (surface mount devices) include vapor phase (VPR), infrared (IR), hot-air convection, or a combination. Wave soldering is mainly used for PTH (plated through-hole) components such as DIP's and discretes, and is sometimes required for SMD when other methods are not feasible. Solder reflow profiles should be properly designed and evaluated by the PCB assembly process engineer based on solder paste, heating method, PCB design, and component sensitivity. Typical solder reflow profiles are illustrated in the following diagrams (Figs 1a and 1b). Critical parameters are heating rate, preheat temperature, duration at the preheat temperature, peak temperature, and cooling rate.

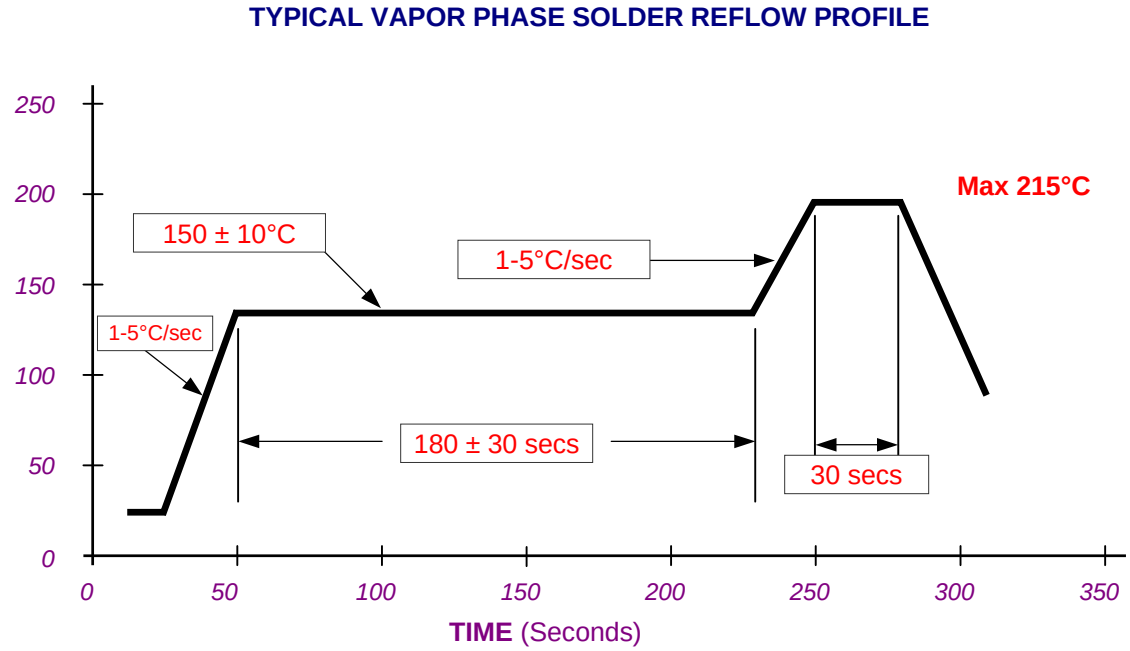


Figure 1a Typical VPR Profile

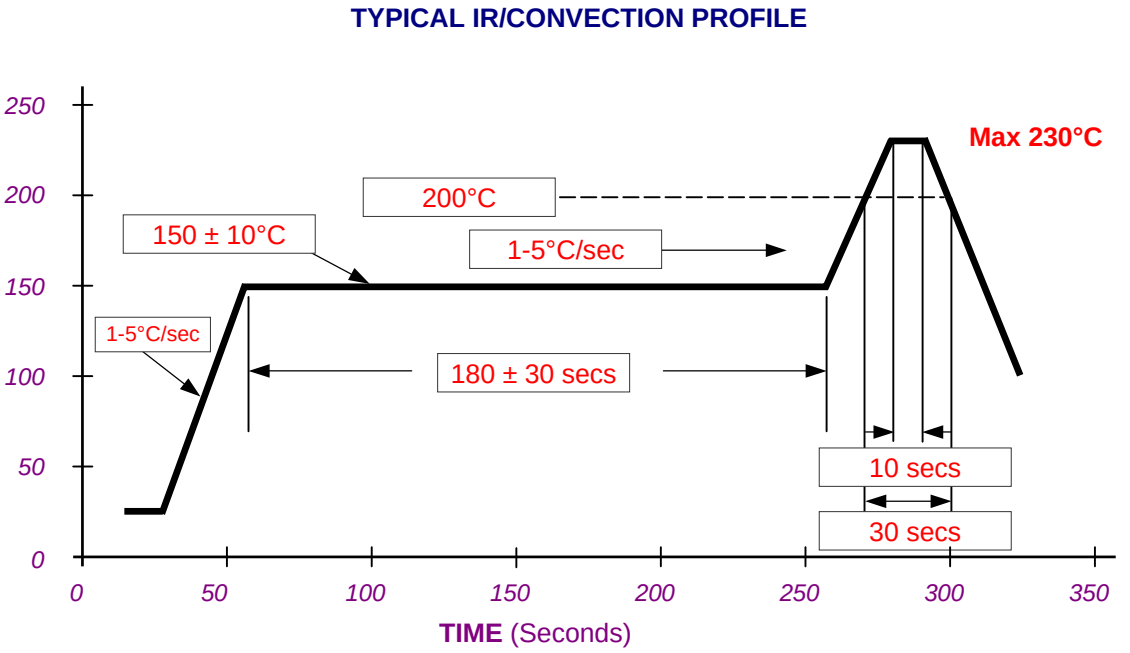


Figure 1b Typical IR/Convection Profile

Note: For typical Pb-free reflow profile, add 15°C to VPR peak-temp and 20°C to IR/convection peak temperature; also, raise preheat temperature by 5°C.

5.4 LEAD-FREE SOLDER

Pb-free lead finish is generally compatible with conventional Sn-Pb (e.g. 63Sn/37Pb, 60Sn/40Pb) and the new Pb-free solder pastes (e.g. Sn-Ag-Cu or Sn-Ag-Cu-Bi alloys). Exar has adopted and qualified matte Sn as standard Pb-free lead finish for all plastic leaded packages (PDIP, SO, PLCC, SSOP, TSSOP, QFP, LQFP, TQFP) and Sn/Ag/Cu solder ball for array packages (e.g. TBGA, EBGA, STBGA, PBGA). The exact solder reflow condition depends on the type and composition of the selected solder paste for PCB assembly. The PCB assembler and/or solder paste vendor shall be consulted for specific processing and cleaning recommendations. It should be noted that the solder joint property is largely determined by the solder paste rather than the lead finish, except in the case of ball array packages (e.g. BGA, CSP).

5.5 MANUAL REWORK & HAND SOLDER REFLOW

Using a soldering iron to perform rework or touchup requires an understanding of the characteristics of the soldering iron, heat input, fluxing, and solder. Although moisture sensitivity and direct heat effect may not be as critical as other solder reflow methods, ESD protection needs to be specifically considered. Soldering irons may generate voltage spikes and damage voltage-sensitive devices such as those containing MOS structures, including CMOS.

The working temperature zone is typically around 330°C+/-15°C. Molten solder needs to be created between the iron tip and component leads to form a solder fillet. Liquid flux can be used as a “heat cushion” to minimize heat damage in the surrounding PCB area. The critical time is when solder is still in the molten stage, which is about 1+/-0.25 seconds. That is also the time when the board is above its glass transition temperature, during which pad lifting or board delamination may occur.

5.6 THERMAL STRESS

IC components are subject to thermal stress as a result of TCE (Temperature coefficient of expansion) mismatch within the package during PCB assembly process. Care should be exercised to ensure that a component’s maximum tolerance is not exceeded, otherwise its intended design capabilities may be compromised. Thermal shock can be minimized by restricting maximum temperature gradients (i.e. heating and cooling rates), and by applying a preheat transition.

5.7 MARK PERMANENCY

Ink marking on package surfaces can be affected and/or degraded by the solvents used in flux rinsing and result in faded or erased marking. Ink adhesion on packages is verified and controlled by means of a Resistance to Solvents test that involves three different chemical mixtures, including A) isopropyl alcohol/mineral spirits, B) terpene based solvent, and C) de-ionized water/propylene glycol monomethyl ether/monoethanolamine, as defined in the suppliers applicable spec. Laser mark is one alternative to ink mark. Although the visual contrast is not as sharp as ink mark, laser mark has been used in the IC industry for some time. The laser mark can minimize handling damage during assembly processing. Therefore, it is considered to be a preferred marking method from a manufacturing point of view. Mark permanency (solvent resistance) is not an issue for laser mark, because it is also considered acceptable from a visual and vision legibility standpoint.

5.8 MOISTURE-RELATED POPCORNING

It is imperative that a PCB assembler be aware of a phenomenon known as the “*popcorn effect*”, or “*popcorning*”. Popcorning is a mechanical failure that can occur in plastic packages during solder reflow. (Refer to Fig. 2 for a failure illustration.) The detrimental effect has been attributed to the moisture accumulated at the interfaces within

package bodies, e.g. interfaces between die and mold compound, mold compound and lead frame or die attach area. The rapid temperature rise from the solder reflow operation causes sudden moisture vaporization at those interfaces. The resulting internal pressure can be sufficient to cause areas of weak adhesion to break or "*delaminate*", resulting in internal and/or external cracking eventually. Even without the package cracking, the interfacial delamination can still cause instant interconnect failure, such as die cracking and wire bond breakage, to occur. Long-term reliability can also be compromised as the result of delamination. Exar's reliability tests for plastic encapsulated products include initial "preconditioning" to simulate the popcorning effect that a part will normally experience during the PCB assembly process.

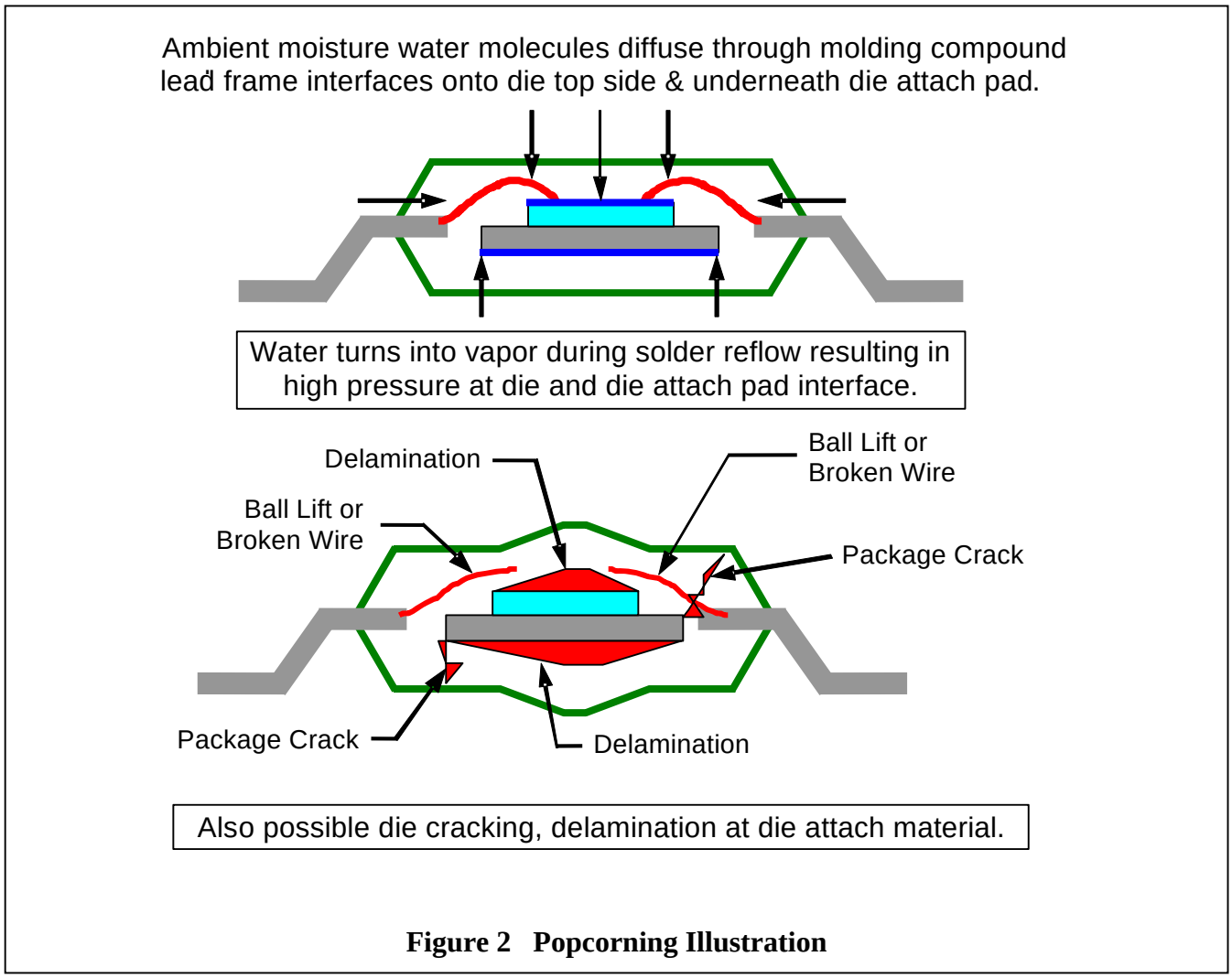


Figure 2 Popcorning Illustration

The key to avoid popcorning is to keep the package dry so that the internal moisture content is below a certain threshold level immediately before solder reflow. Common remedies include:

- Bake and dry pack products prior to shipping.
- Pre-bake parts immediately before PCB assembly or solder reflow.
- Use improved mold compounds that provide greater moisture resistance, better adhesion, and higher mechanical strength.

5.9 MOISTURE SENSITIVITY LEVELS

JEDEC MSL Classification

According to the latest EIA/JEDEC Standard 020C, moisture sensitivity can be classified into 8 different levels: 1, 2, 2a, 3, 4, 5, 5a, and 6, with level 6 being the most sensitive. Maximum floor life after opening of the dry pack is specified for each level as recommended by JEDEC. The MSL is classified in relation to preconditioning conditions that simulate moisture soaking in common ambient and reflow conditions.

MSL	***Preconditioning***			***Max. Floor Life***			***Recommended Rebake***
	°C	*RH%*	*Hours*	*°C*	*RH%*	*Time*	*Temperature / Time*
1	85	85	168	30	85	unlimited	None
2	85	60	168	30	60	1year	125°C / 12hours
2a	30	60	696	30	60	4weeks	125°C / 12hours
3	30	60	192	30	60	1week	125°C / 12hours
4	30	60	96	30	60	72hours	125°C / 24hours
5	30	60	72	30	60	48hours	125°C / 24hours
5a	30	60	48	30	60	24hours	125°C / 24hours
6	30	60	as specified	30	60	as specified	125°C / 24hours

(Source: JEDEC-STD-020C, www.jedec.org)

It should be noted here that the JEDEC MSL standard is based on some additional test conditions described as follows:

- Reflow peak temperature: 240°C, 10 seconds for small packages with a volume < 350mm³ and thickness <2.5mm³; 225°C, 10 seconds for other packages, including all BGAs.
- Reflow heating rate: 5°C/sec max.
- Moisture loading: refer to the preconditioning table above.
- PCB manufacturing ambient: 30°C/60RH% max is recommended.

If actual reflow conditions or manufacturing environment are harsher than specified, some downgrade adjustments on maximum floor life or MSL may be necessary. Please contact Exar's sales representative for your special application or requirement.

MSL of Exar Packages (subject to change based on rel data update)

PACKAGE	PACKAGE CONFIGURATION	Sn-Pb/ Pb-Free	Package Peak Reflow Temp
JEDEC SOIC/SOJ/QSOP	0.150”	1	260C
JEDEC SOIC/SOJ	0.300”	1	260C
EIAJ SOP	4.4, 5.3, 5.4, 7.8, 8.4mm	1	260C
SSOP	5.3mm	1	260C
TSSOP	4.4, 6.1mm	1	260C
PLCC	20, 28, 32, 44lds	1	260C
	52, 68, 84lds	1	260C
QFP	10x10mm	1	260C
	>10x10mm	2a	250C
	>20x20mm	4	250C
LQFP (1.4mm thick)	7x7mm	1	260C
	>7x7mm	2a	260C
	>20x20 mm	4	260C
TQFP (1.0mm thick)	7x7mm	1	260C
	>7x7mm	2a	260C
	>20x20 mm	4	260C
Leaded TEP (Thermal-Enhanced Packages)	All	4	250C
All BGA’s	All	4	245C
QFN	Up to 5x5mm	1	260C
	Up to 9x9mm	2a	260C

Note: 1) The package MSL depends on material, process, die, lead frame, and the actual MSL test conditions. The above table is for general reference only based on Exar’s latest reliability test data.
2) Max reflow peak temperatures are per latest Jedec std 020.
3) Thermal enhancements for TEP include attached heat slug, drop-in heat spreader, exposed pad, and etc.

Dry-Pack MSL Labeling

Exar realizes that not all end users or PCB assemblers are able to operate under the environmental conditions with maximum temperature and humidity as defined in Jedec MSL classification. To compensate for possible excessive out-of-standard storage or floor condition, Exar considers that it is appropriate to reduce MSL by one level for dry-pack labeling in order to preserve adequate safety margin. This also covers those lot-to-lot variations in materials, processes, and the statistical uncertainty in the sampling reliability testing. Please refer to the MSL table in the last section for a comparison.

5.10 COPLANARITY

Lead integrity is critical to the quality of solder joints during the PCB assembly process, and is commonly judged by the degree of bent lead and, more often, coplanarity. Coplanarity is defined as the maximum distance between the seating plane and individual leads of a given SMT device. Refer to Fig. 3 for illustration.

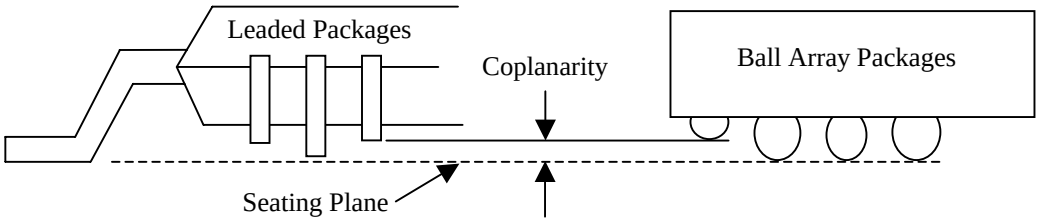


Fig. 3 Coplanarity Illustration

Continuity failures (open circuit) may occur if coplanarity exceeds 0.006" for lead pitch >0.5mm or 0.004" for fine-pitch packages. Exar follows JEDEC Publication 95 for coplanarity criteria listed in the table below.

PACKAGE TYPE	LEAD PITCH	MAX COPLANARITY
SOIC, SOJ, PLCC	1.27mm (0.050")	0.1mm (0.004")
SSOP, TSSOP	≥0.65mm (0.0256")	0.1mm (0.004")
TSSOP	≤ 0.5mm (0.0197")	0.08mm (0.0031")
QFP, LQFP, TQFP	> 0.5mm (0.0197")	0.1mm (0.004")
QFP, LQFP, TQFP	≤ 0.5mm (0.0197")	0.08mm (0.0031")
BGA	≤ 0.8mm (0.0315") ≥ 1.0mm (0.0394")	0.15mm (0.0059") 0.2mm (0.0079")

Reference: EIA/JEDEC Publication 95

6.0 ESD HANDLING AND CLASSIFICATION

6.1 ESD (Electrostatic Discharge) MODELS & TEST METHODS

There are three common ESD models to represent the origin of an ESD event that may occur in the field.

1. Human Body Model (HBM, "100pF, 1.5K Ohms"): the oldest and most commonly used. This model simulates the discharge from the fingertip of a standing individual delivered to the device.

2. Machine Model (MM, "200pF, Zero Ohm"):

   This model simulates an automated assembly and manufacturing environment.

3. Field-Induced Charged-Device Model (CDM):

   This model is difficult to reproduce in practice; however, it is the most important model for modern automated assembly and manufacturing environments. This model represents the event where mobile and immobile charges are generated on the component and a very rapid discharge occurs after the component touches a conductive surface. Typical event cycle time is 100-500 psec.

ESD Test Methods

The following industry standards can be referred to for further details.

1. EIA/JEDEC Standard A114 "ESD Sensitivity Testing HBM" (human body model)

2. EIA/JEDEC Standard A115 "ESD Sensitivity Testing MM" (machine model)

3. JEDEC Standard JESD22-C101 "Field-Induced Charged-Device Model" (CDM)

4. ANSI EOS/ESD S5.1 (HBM), S5.2 (MM), and DS5.3 (CDM)

   Note: A114, A115, and C101 are downloadable from JEDEC

Exar Standard ESD Rating

Exar applies the following minimum ESD rating to all standard products unless otherwise specified:

2000 volts HBM

6.2 ESD Protection and Handling Precaution

ESD Protection

Exar uses only ESD-safe materials for packing and shipping. Shipping tubes for DIP/PLCC/SO have an anti-static coating layer; shipping trays for QFP's are conductive; chip trays for die sales are either conductive or static-dissipative; shipping bags are static-dissipative; tape & reel materials are conductive or static-dissipative.

Handling Precautions

IC components are sensitive to ESD damage. Extreme care should be exercised when handling parts. Machines, tools, and personnel should be properly grounded by using appropriate grounding or ESD-protection devices.

7.0 PACKING, SHIPPING AND STORAGE

7.1 DRY PACK

Exar has implemented bake and dry pack for those packages that have been determined to be moisture-sensitive and failure-prone, except for MSL-1 devices. Bake involves oven-baking at 125°C for a specified duration, while dry pack employs a moisture barrier bag with baked devices, desiccant, and humidity indicator card sealed inside the bag, preventing external moisture from getting into the devices. Refer to Fig. 4 for dry pack illustration. Typical shelf life for dry-packed devices is 12 months from the seal date. Seal date, handling procedure, and rebake recommendation are available on the warning label on each dry-pack bag. The humidity indicator card provides information on the condition of the dry-pack bag and moisture inside the bag. (Refer to section 7.2 for further information on the humidity indicator card).

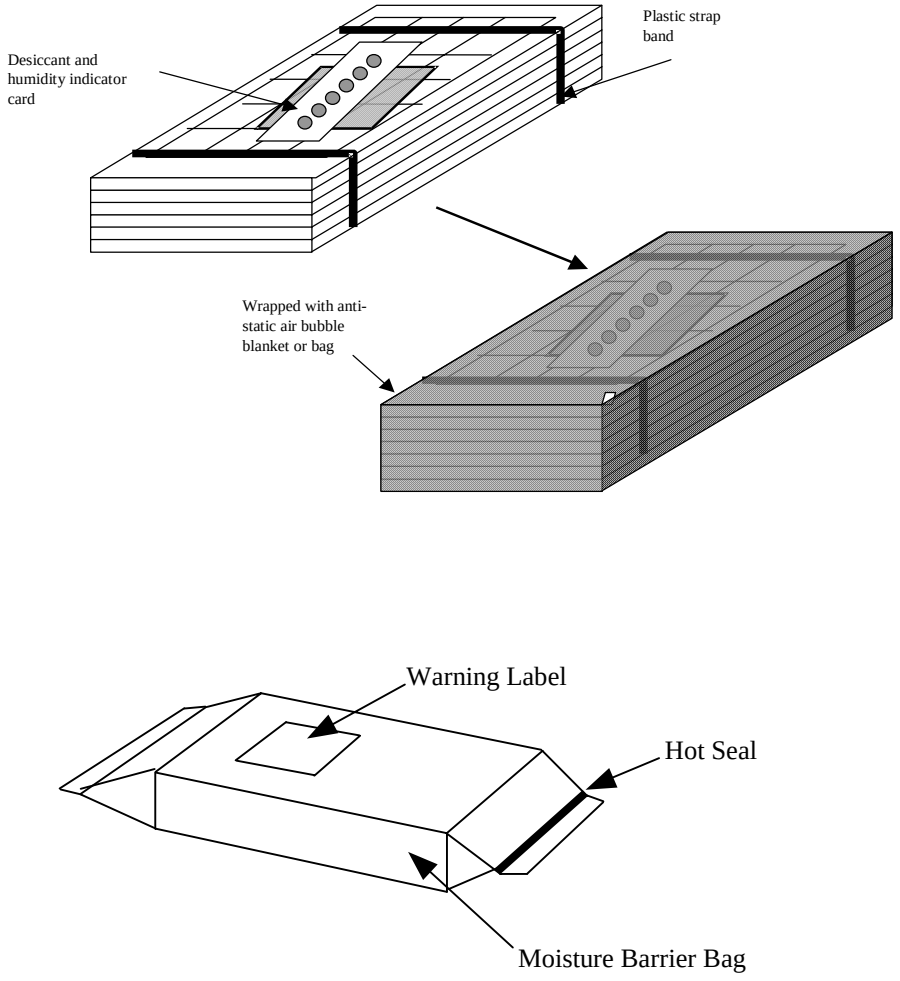


Figure 4 Dry Pack (Inside Moisture-Barrier Bag)

7.2 HUMIDITY INDICATOR CARD

A humidity indicator card (HIC) is included in each dry-pack bag to monitor the moisture content inside the bag. It should be noted that typical shelf life is 12 months for a standard dry pack under normal storage environment (<35C and <75%RH). After 12 months, the moisture content inside packages may become questionable and verification or rebake may be necessary. The humidity indicator card can show if the moisture (humidity) inside the dry-pack bag has reached or exceeded the "danger" level as specified on the card. If so, the parts should be re-baked. The HIC can also alert users when there is any damage (e.g. puncture) to the moisture-barrier bags. Refer to Fig. 5 for HIC illustration.

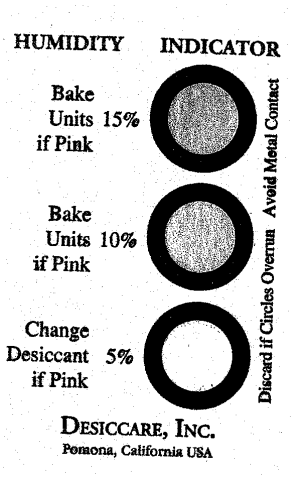


Fig. 5 Humidity Indicator Card

7.3 PACKAGE ORIENTATION

- *Tube:* pin #1 towards tube opening; applicable packages: DIP, SO (including SOIC, SOP, SSOP, QSOP, TSSOP), PLCC, QFN.
- *Tray:* pin #1 towards JEDEC-tray chamfered corner; applicable packages: QFP (including LQFP, TQFP), BGA, QFN.
- *Tape & Reel:* pin #1 towards sprocket hole; applicable packages: PLCC, SO, QFP, BGA.

Refer to Fig. 6 below for illustration.

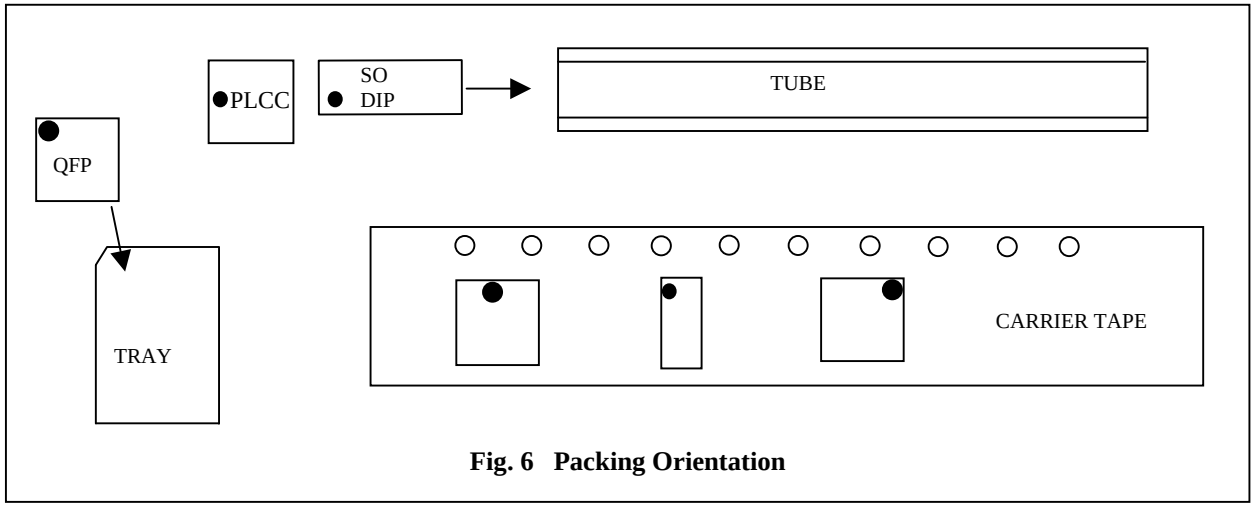
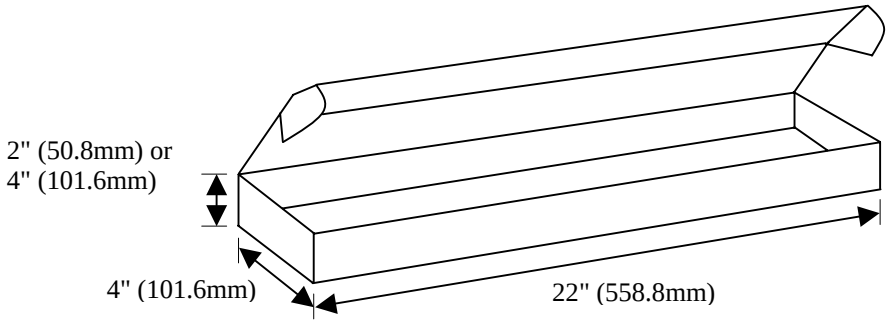


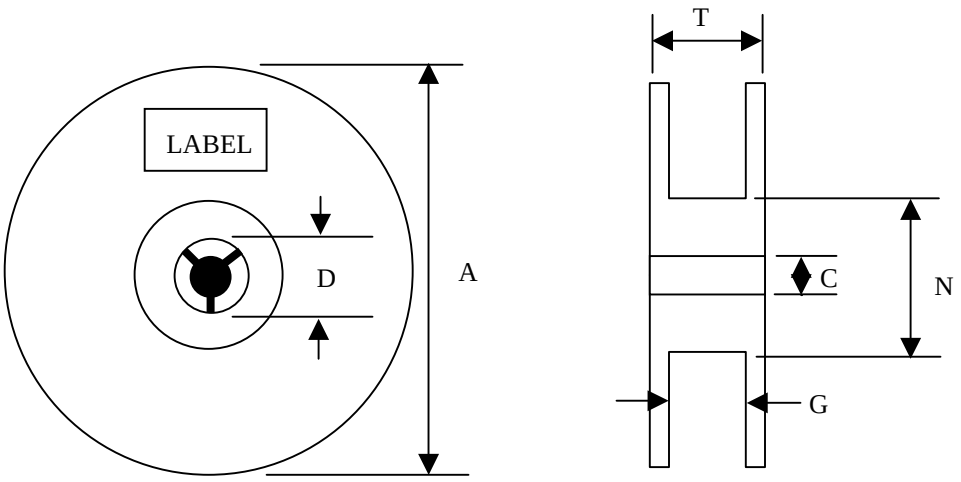
Fig. 6 Packing Orientation

7.4 SHIPPING CONTAINER DIMENSIONS

SHIPPER	DIMENSION
Tube (DIP, PLCC, SOIC, SOJ, SSOP, TSSOP)	20" +/-0.5" (508 +/-12.7 mm)
Tube (EIAJ 4.4mm SOP)	280 +/-3 mm
Tube (EIAJ 5.4mm SOP)	400 +/-3 mm
Tube (EIAJ 7.8/8.4mm SOP)	495 +/-3 mm
Tube (32ld SDIP)	460 +/-3 mm
JEDEC Low-Profile Metric Tray (QFN, QFP, LQFP, TQFP)	135.9x315.0x7.62t +/-0.25 mm
Carrier Tape	By package (see next table)
Cover Tape	By package (see next table)
Reel	13" diameter (330.2 mm diameter)
Inner Box - medium	4"x4"x22" +/-0.5" (101.6 x 101.6 x 558.8 +/-12.7 mm)
Inner Box - small	2"x4"x22" +/-0.5" (50.8 x 101.6 x 558.8 +/-12.7 mm)



Inner Box Dimension

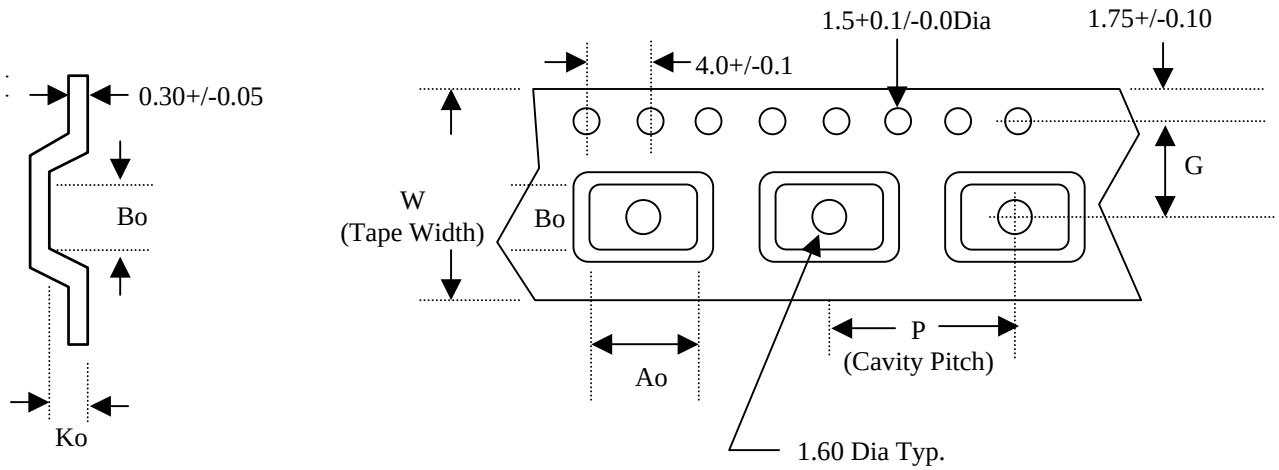


Tape Size	A	C	D min	N min	G	T Max
12mm	13.0”	.512”+/-.008”	0.795”	1.97”	.448” +.079”/-.00	.724”
mm->	*330.2*	*13+/-0.2*	*20.2*	*50.0*	*11.4 +2.0/-0.0*	*18.4*
16mm	13.0”	.512”+/-.008”	0.795”	1.97”	.646” +.079”/-.00	.882”
mm->	*330.2*	*13+/-0.2*	*20.2*	*50.0*	*16.4 +2.0/-0.0*	*22.4*
24mm	13.0”	.512”+/-.008”	0.795”	1.97”	.961”+.079”/-.00	1.20”
mm->	*330.2*	*13+/-0.2*	*20.2*	*50.0*	*24.4 +2.0/-0.0*	*30.5*
32mm	13.0”	.512”+/-.008”	0.795”	1.97”	1.28” +.079”/-.00	1.51”
mm->	*330.2*	*13+/-0.2*	*20.2*	*50.0*	*32.5 +2.0/-0.0*	*38.4*
44mm	13.0”	.512”+/-.008”	0.795”	1.97”	1.75” +.079”/-.00	1.98”
mm->	*330.2*	*13+/-0.2*	*20.2*	*50.0*	*44.4 +2.0/-0.0*	*50.3*

Note: 1) Actual T dimension depends on carrier tape width.
2) Typical N dimensions are 4” (101.6mm) or 7” (177.8mm).

Reel Dimension

Typical Carrier Tape Dimension Illustration



UNIT: mm

Notes:
1) Cavity features are manufacturer's option.
2) Two-sided sprocket hole design is employed for tapes > 24mm in width.
3) Refer to the next page for detailed tape dimension table.

Typical Carrier Tape Dimension Table

Package	Dimensions (Unit: mm)					
	W	P	Ao	Bo	Ko	G
8ld JEDEC SOIC(.150")	12	8	6.4	5.2	2.1	5.5+/-0.05
14ld JEDEC SOIC(.150")	16	8	6.5	9.5	2.1	7.5+/-0.1
16ld JEDEC SOIC(.150")	16	8	6.5	10.3	2.1	7.5+/-0.1
16ld JEDEC SOIC(.300")	16	12	10.9	10.7	3.0	7.5+/-0.1
18ld JEDEC SOIC(.300")	24	12	10.9	12.0	3.0	11.5+/-0.1
20ld JEDEC SOIC(.300")	24	12	10.9	13.3	3.0	11.5+/-0.1
24ld JEDEC SOIC(.300")	24	12	10.9	16.0	3.0	11.5+/-0.1
28ld JEDEC SOIC(.300")	24	16	10.9	18.5	3.0	11.5+/-0.1
20ld SOJ(.300")	24	12	9.0	13.5	3.7	11.5+/-0.1
24ld SOJ(.300")	24	12	9.1	16.3	4.0	11.5+/-0.1
28ld SOJ(.300")	24	12	9.3	18.8	4.0	11.5+/-0.1
8ld EIAJ SOP(4.4mm)	12	8	7.1	6.0	2.1	5.5+/-0.1
8ld EIAJ SOP(4.4mm) special	12	12	6.7	5.4	2.1	5.5+/-0.1
18ld EIAJ(5.4mm)	24	12	8.2	11.6	2.5	11.5+/-0.1
22ld EIAJ SOP(5.4mm)	24	12	8.6	14.5	2.2	11.5+/-0.1
24ld EIAJ SOP(5.4mm)	24	12	8.6	15.8	2.2	11.5+/-0.1
28ld EIAJ SOP(7.5mm)	24	16	12.5	18.7	2.7	11.5+/-0.1
28ld EIAJ SOP(8.4mm)	24	16	12.3	18.8	3.0	11.5+/-0.1
20ld SSOP(5.3mm)	16	12	8.2	7.5	2.5	7.5+/-0.1
24ld SSOP(5.3mm)	24	12	8.2	8.8	2.5	11.5+/-0.1
28ld SSOP(5.3mm)	24	12	8.4	10.9	2.4	11.5+/-0.1
28TSSOP(4.4mm)	24	12	6.8	10.1	1.6	11.5+/-0.1
48TSSOP(6.1mm)	24	12	8.6	13.0	1.8	11.5+/-0.1
20ld PLCC	16	12	10.3	10.3	4.9	11.5+/-0.1
28ld PLCC	24	16	13.0	13.0	4.9	11.5+/-0.1
32ld PLCC	24	16	13.0	15.5	4.9	11.5+/-0.1
44ld PLCC	32	24	18.0	18.0	4.9	14.2+/-0.1
52ld PLCC	32	24	20.5	20.5	5.8	14.2+/-0.1
68ld PLCC	44	32	25.6	25.6	5.8	20.2+/-0.15
84ld PLCC	44	36	30.7	30.7	5.8	20.2+/-0.15
44/52 QFP (10x10x2.0mm)	24	24	16.6	16.6	1.8	11.5+/-0.1
32ld LQFP(7x7x1.4mm)	16	12	9.6	9.6	2.0	7.5+/-0.1
48ld LQFP(7x7x1.4mm)	16	12	9.6	9.6	2.0	7.5+/-0.1
48ld TQFP(7x7x1.0mm)	16	12	9.6	9.6	1.5	7.5+/-0.1
44/52/64ld LQFP(10x10x1.4mm)	24	16	9.5	9.5	2.0	11.5+/-0.1
80/100/120/128ld LQFP(14x14x1.4mm)	24	20	16.5	16.5	2.0	11.5+/-0.1
100ld TQFP (14x14x1.0mm)	24	24	16.25	16.3	1.75	11.5+/-0.1
120/128 LQFP (14x20x1.4mm)	44	24	16.5	22.5	2.0	20.2+/-0.15
144 LQFP (20x20x1.4mm)	44	32	22.5	22.5	2.0	20.2+/-0.15
272PBGA (27x27x2.15mm)	44	32	27.5	27.5	2.9	20.2+/-0.15
352/388PBGA (35x35x2.15mm)	56	40	35.5	35.5	2.8	26.2+/-0.15
504TBGA(35x35x0.9mm)	56	40	35.4	35.4	3.2	26.2+/-0.15

Notes: 1) "LQFP" also refers to "TQFP-1.4mm" and "TQFP" refers to "TQFP-1.0mm".
2) Some refer both TQFP-1.4mm and TQFP-1.0mm as to "TQFP".
3) Please double check package thickness to identify "LQFP" and "TQFP" correctly.

7.5 PACKING QUANTITY

Refer to the following table for general reference on packing quantity of tube/tray/tape&reel/dry pack.

SOIC/SOP/SOJ/SSOP/TSSOP/QSOP/PLCC/QFN Packing Quantity Table

PKG CODE	PIN	EXAR Standard Package Description	Package Qty			Per Box/Bag Qty		
			Tube	Tray	Reel	Small	Medium	Dry Bag
D8	8	8ld JEDEC SOIC (.150")	97	-	2500	100	200	-
D14	14	14ld JEDEC SOIC (.150")	56	-	2500	100	200	-
D16	16	16ld JEDEC SOIC (.300")	46	-	1000	75	100	-
DB16	16	16ld JEDEC SOIC (.150")	48	-	2500	100	200	-
D18	18	18ld JEDEC SOIC (.300")	41	-	1000	75	100	-
D20	20	20ld JEDEC SOIC (.300")	37	-	1000	75	100	-
D24	24	24ld JEDEC SOIC (.300")	31	-	1000	75	100	-
D28	28	28ld JEDEC SOIC (.300")	27	-	1000	75	100	-
DB28	28	28ld JEDEC SOIC (.350")	25	-	-	75	100	-
G20	20	20ld JEDEC TSSOP (4.4mm)	74	-	2500	150	300	-
G24	24	24ld JEDEC TSSOP (4.4mm)	62	-	2500	150	300	-
G28	28	28ld JEDEC TSSOP (4.4mm)	50	-	2500	150	300	-
G38	38	38ld JEDEC TSSOP (4.4mm)	50	-	2500	150	300	-
G48	48	48ld JEDEC TSSOP (6.1mm)	39	-	-	150	300	-
J20	20	20ld JEDEC PLCC	49	-	1000	40	80	-
J28	28	28ld JEDEC PLCC	38	-	750	40	80	-
J32	32	32ld JEDEC PLCC	32	-	750	40	80	-
J44	44	44ld JEDEC PLCC	27	-	500	20	40	-
J52	52	52ld JEDEC PLCC	24	-	500	20	40	-
J68	68	68ld JEDEC PLCC	19	-	250	15	35	-
J84	84	84ld JEDEC PLCC	16	-	250	15	30	-
K24	24	24ld EIAJ SOP (5.4mm)	32	-	1000	75	150	-
L16	16	16pad JEDEC QFN (4X4mm)	-	490	2500	100	200	-
L20	20	20pad JEDEC QFN (4x4mm)	-	490	2500	100	200	-
L32	32	32pad JEDEC QFN (5x5mm)	-	490	2500	100	200	-
L40	40	40pad JEDEC QFN (6x6mm)	-	490	2500	100	200	-
L48	48	48pad JEDEC QFN (7x7mm)	-	260	2500	100	200	-
L64	64	64pad JEDEC QFN (9x9mm)	-	260	1500	100	200	-
R24	24	24ld QSOP (.150")	56	-	2500	150	300	-
R28	28	28ld QSOP (.150")	46	-	2500	150	300	-
U20	20	20ld JEDEC SSOP (5.3mm)	66	-	1000	50	75	-
U24	24	24ld JEDEC SSOP (5.3mm)	58	-	1000	50	75	-
U28	28	28ld JEDEC SSOP (5.3mm)	47	-	1000	50	75	-
W20	20	20ld JEDEC SOJ (.300")	37	-	1000	50	75	-
W28	28	28ld JEDEC SOJ (.300")	27	-	1000	50	75	-

Notes: 1) Box/Bag quantity is for general reference only and indicates the number of tubes per box or trays per bag. The actual quantity depends on actual box size and drop-ship requirements.

QFP/LQFP/TQFP Packing Quantity Table

Pkg Code	Pin	EXAR Standard Package Description	Package Qty			Per Box/Bag Qty		
			Tube	Tray	Reel	Small	Medium	Dry Bag
QB32	32	32ld JEDEC (L)QFP (7x7x1.4mm) 1.0mm form	-	250	1500	-	-	6
Q44	44	44ld JEDEC QFP (10x10x2.0mm) 1.6mm form	-	96	1000	-	-	6
QC44	44	44ld JEDEC QFP (10x10x2.0mm) 1.95mm form	-	96	1000	-	-	6
QD44	44	44ld JEDEC QFP (14x14x2.7mm) 1.6mm form	-	84	500	-	-	6
Q52	52	52ld JEDEC QFP (10x10x2.0mm) 1.6mm form	-	96	1000	-	-	6
QD52	52	52ld JEDEC QFP (10x10x2.0mm) 1.95mm form	-	84	1000	-	-	6
Q64	64	64ld JEDEC QFP (14x14x2.7mm) 1.6mm form	-	84	500	-	-	6
QB64	64	64ld JEDEC QFP (10x10x2.0mm) 1.6mm form	-	96	1000	-	-	6
Q80	80	80ld JEDEC QFP (14x14x2.7mm) 1.6mm form	-	84	500	-	-	6
Q100	100	100ld JEDEC QFP (14x20x2.8mm) 1.6mm form	-	66	500	-	-	6
QB100	100	100ld JEDEC QFP (14x20x2.8mm) 1.95mm form	-	66	400	-	-	6
Q160	160	160ld JEDEC QFP (28x28x3.5mm) 1.6mm form	-	24	250	-	-	6
Q208	208	208ld JEDEC QFP (28x28x3.5mm) 1.3mm form	-	24	250	-	-	6
V44	44	44ld JEDEC LQFP (10x10x1.4mm) 1.0mm form	-	160	1000	-	-	6
VB48	48	48ld JEDEC QFP (7x7x1.4mm) 1.0mm form	-	250	1500	-	-	6
M48	48	48ld JEDEC TQFP (7x7x1.0mm) 1.0mm form	-	250	1500	-	-	6
M100	100	100ld JEDEC TQFP (14x14x1.0mm) 1.0mm form	-	90	1000	-	-	6
V52	52	52ld JEDEC LQFP (10x10x1.4mm) 1.0mm form	-	160	1000	-	-	6
V64	64	64ld JEDEC LQFP (10x10x1.4mm) 1.0mm form	-	160	1000	-	-	6
V80	80	80ld JEDEC LQFP (14x14x1.4mm) 1.0mm form	-	90	1000	-	-	6
VB80	80	80ld JEDEC LQFP-TEP (14x14x1.4mm) 1.0mm form	-	90	1000	-	-	6
V100	100	100ld JEDEC LQFP (14x14x1.4mm) 1.0mm form	-	90	1000	-	-	6
V120	120	120ld JEDEC LQFP-TEP (14x14x1.4mm) 1.0mm form	-	90	1000	-	-	6
VB120	120	120ld JEDEC LQFP-TEP (14x20x1.4mm) 1.0mm form	-	72	1000	-	-	6
V128	128	128ld JEDEC LQFP-TEP (14x14x1.4mm) 1.0mm form	-	90	1000	-	-	6
VB128	128	128ld JEDEC LQFP-TEP (14x20x1.4mm) 1.0mm form	-	72	1000	-	-	6
V144	144	144ld JEDEC LQFP (20x20x1.4mm) 1.0mm form	-	60	750	-	-	6
VB144	144	144ld JEDEC LQFP-TEP (20x20x1.4mm) 1.0mm form	-	60	750	-	-	6
V208	208	208ld JEDEC LQFP (28x28x1.4mm) 1.0mm form	-	36	250	-	-	6
VB208	208	208ld JEDEC LQFP-TEP (28x28x1.4mm) 1.0mm form	-	36	250	-	-	6

Notes: 1) Dry pack per-bag qty includes one cover tray.
2) "TEP": thermal enhanced package (including a variety of thermal enhancement designs).
3) Box/Bag quantity is for general reference only and indicates the number of tubes per box or trays per bag. The actual quantity depends on actual box size and drop-ship requirements.

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BGA Packing Quantity Table

Pkg Code	Pin	EXAR Standard Package Description	Package Qty			Per Box/Bag Qty		
			Tube	Tray	Reel	Small	Medium	Dry Bag
B196	196	196Ball STBGA (12x12x2.15mm, 14x14matrix)0.8mm pitch	-	168	1000	-	-	6
B208	208	208Ball STBGA (17x17x2.15mm, 16x16matrix)1.0mm pitch	-	90	500	-	-	6
B217	217	217Ball PBGA (23x23x2.15mm, 17x17matrix)1.27mm pitch	-	60	500	-	-	6
B225	225	225Ball PBGA (19x19x2.15mm, 18x18matrix)1.0mm pitch	-	84	500	-	-	6
B272	272	272Ball PBGA (27x27x2.15mm, 20x20matrix)1.27mm pitch	-	40	400	-	-	6
B289	289	289Ball PBGA (15x15x2.15mm, 17x17matrix)0.8mm pitch	-	126	1000	-	-	6
B304	304	304Ball PBGA (31x31x2.15mm, 30x30matrix)1.00mm pitch	-	27	400	-	-	6
B316	316	316Ball PBGA (21x21x2.15mm, 20x20matrix)1.00mm pitch	-	60	500	-	-	6
B352	352	352Ball PBGA (35x35x2.15mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
B388	388	388Ball PBGA (35x35x2.15mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
B420	420	420Ball PBGA (35x35x1.0mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
B456	456	456Ball PBGA (27x27x2.15mm, 26x26matrix)1.00mm pitch	-	40	400	-	-	6
B484	484	484Ball PBGA (23x23x2.15mm, 22x22matrix)1.00mm pitch	-	40	400	-	-	6
BB304	304	304Ball TBGA (31x31x1.0mm, 30x30matrix)1.00mm pitch	-	27	400	-	-	6
BB396	396	396Ball TBGA (37.5x37.5x1.0mm, 36x36matrix)1.0mm pitch	-	21	300	-	-	6
BB420	420	420Ball TBGA (35x35x0.9mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
BB504	504	504Ball TBGA (35x35x0.9mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
BB584	584	584Ball TBGA (37.5x37.5x0.9mm, 27x27matrix)1.27mm pitch	-	21	300	-	-	6
BC516	516	516Ball PBGA-TEP (35x35x2.15mm, 26x26matrix)1.27mm pitch	-	24	350	-	-	6
BC568	568	568Ball PBGA-TEP (31x31x2.15mm, 30x30matrix)1.00mm pitch	-	27	400	-	-	6
BC780	780	780Ball PBGA-TEP (37.5x37.5x0.9mm, 36x36matrix)1.00mm pitch	-	21	300	-	-	6
BF1397	1397	1397Ball FCBGA (40x40x2.5mm, 39x39matrix)1.00mm pitch	-	21	-	-	-	6

Notes: 1) Dry pack per-bag qty includes one cover tray.
2) "TEP": thermal enhanced package (including a variety of thermal enhancement designs).
3) Box/Bag quantity is for general reference only and indicates the number of tubes per box or trays per bag. The actual quantity depends on actual box size and drop-ship requirements.

DIP Packing Quantity Table

Pkg Code	Pin	EXAR Standard Package Description	Package Qty			Per Box/Bag Qty		
			Tube	Tray	Reel	Small	Medium	Dry Bag
N8	8	8ld JEDEC CDIP (. 300")	48	-	-	20	40	-
N14	14	14ld JEDEC CDIP (.300")	25	-	-	20	40	-
N16	16	16ld JEDEC CDIP (.300")	25	-	-	20	40	-
N18	18	18ld JEDEC CDIP (.300")	20	-	-	20	40	-
N20	20	20ld JEDEC CDIP (.300")	20	-	-	20	40	-
N22	22	22ld JEDEC CDIP (.400")	15	-	-	15	30	-
N24	24	24ld JEDEC CDIP (.600")	15	-	-	10	25	-
NB24	24	24ld JEDEC CDIP (.400")	15	-	-	15	30	-
NC24	24	24ld JEDEC CDIP (.300")	15	-	-	15	30	-
N28	28	28ld JEDEC CDIP (.600")	13	-	-	10	25	-
NB28	28	28ld JEDEC CDIP (.300")	-	-	-	15	30	-
N40	40	40ld JEDEC CDIP (.600")	9	-	-	10	25	-
P8	8	8ld JEDEC PDIP (.300")	50	-	-	20	40	-
P14	14	14ld JEDEC PDIP (.300")	25	-	-	20	40	-
P16	16	16ld JEDEC PDIP (.300")	25	-	-	20	40	-
P18	18	18ld JEDEC PDIP (.300")	20	-	-	20	40	-
P20	20	20ld JEDEC PDIP (.300")	18	-	-	20	40	-
P22	22	22ld JEDEC PDIP (.300")	18	-	-	15	30	-
PB22	22	22ld JEDEC PDIP (.400")	17	-	-	15	30	-
P24	24	24ld JEDEC PDIP (.600")	15	-	-	15	30	-
PB24	24	24ld JEDEC PDIP (.300")	15	-	-	10	25	-
PC24	24	24ld JEDEC PDIP (.400")	15	-	-	15	30	-
P28	28	28ld JEDEC PDIP (.600")	13	-	-	10	25	-
PB28	28	28ld JEDEC PDIP (.300")	14	-	-	15	30	-
P40	40	40ld JEDEC PDIP (.600")	9	-	-	10	25	-

Note: 1) Box/Bag quantity is for general reference only and indicates the number of tubes per box or trays per bag. The actual quantity depends on actual box size and drop-ship requirements.

7.6 STORAGE CONDITIONS

- A controlled environment is required for long-term storage of components prior to PCB assembly. For the storage life of components mounted on PCB, please refer to individual product datasheets.
- Typically, 12 months is considered the maximum storage life in an environment of temperature <25°C and humidity <40%RH. Higher temperature and/or higher humidity may shorten the typical storage life. Please consult with Exar Quality Assurance for special requirements.
- Main concerns on long-term storage: solderability degradation and moisture content in packages.

7.7 LABELS

Exar uses various labels to identify contents and provide additional special warnings and/or instructions. For example,

- Packing Label: Show Exar part number, quantity, date code, lot #, test date (Fig. 7a)
- ESD Warning Label: Caution for electrostatic sensitivity (Fig. 7b)
- Moisture Warning Label: Caution for moisture sensitivity, rebake and handling instructions. (Fig. 7c)
  Note: Refer to Jedec standard or section 5.9 table for corresponding recommended floor life.

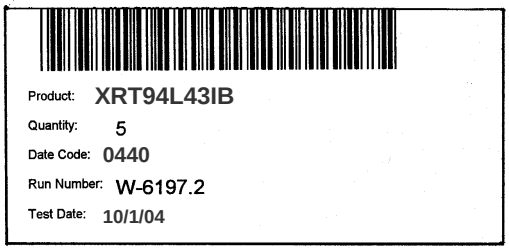


Figure 7a Packing Label

Figure 7b ESD Caution Label

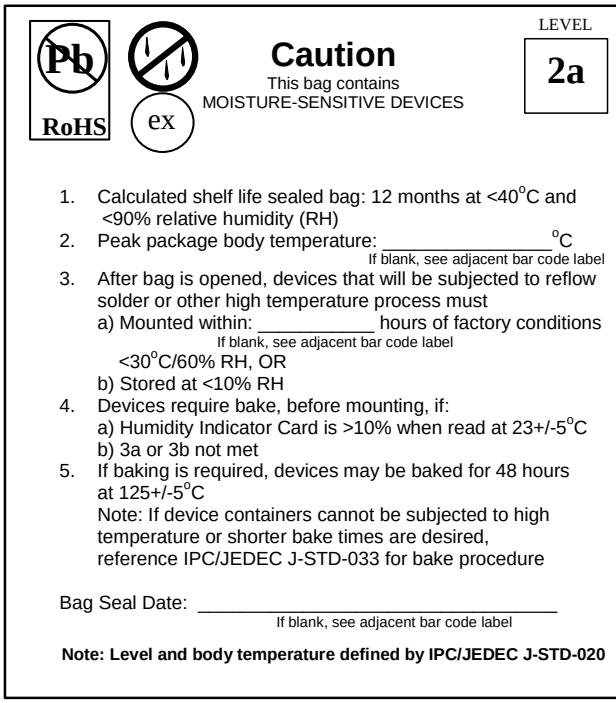


Figure 7c Jedec Moisture Warning Label

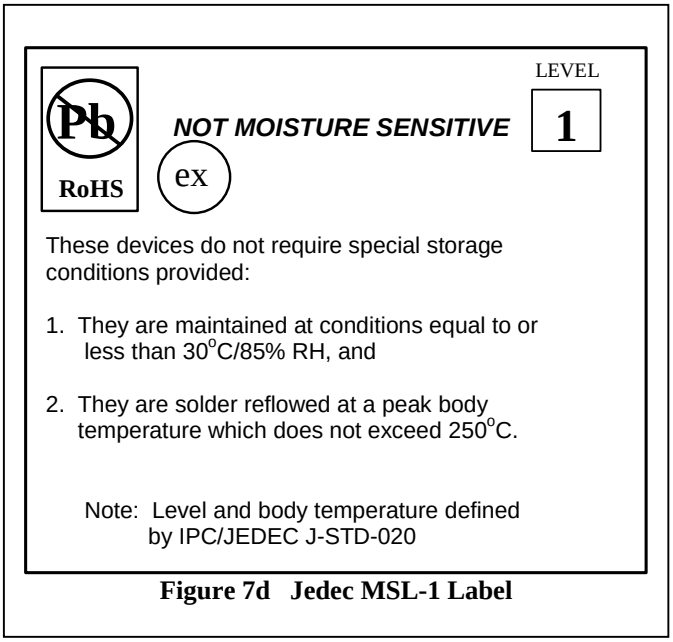


Figure 7d Jedec MSL-1 Label

8.0 THERMAL MANAGEMENT

8.1 WHY THERMAL MANAGEMENT?

Any semiconductor device has a maximum temperature tolerance for desired operating performance and reliability during the product life. Excessive heat degrades device performance and induces chip or package-related field failures. While budgeting power consumption during the design stage, removing heat efficiently and economically at both package and board levels has become a critical consideration in product design.

8.2 JUNCTION TEMPERATURE (T_j)

The critical device temperature is commonly represented by the maximum "junction temperature" of an IC chip. The maximum temperature experienced by a junction (mainly p-n junction) determines whether the IC chip can function properly and meet design specifications.

8.3 THETA ja & jc

There are three major variables that directly affect junction temperature during device operation:

- Power dissipation (P)
- Ambient operating temperature (T_a)
- Package thermal resistance or impedance (θ or theta)

Although not rigorously correct, a simple relationship among the three variables has been used by many to determine if there will be a potential concern about device thermal performance in a given package. The relationship can be expressed as follows.

$$\theta_{ja} = \frac{T_j - T_a}{P_{max}} \qquad \text{similarly, } \theta_{ca} = \frac{T_c - T_a}{P_{max}}$$

* T_c refers to package case temperature, usually top center.

The above expression can be used in several different ways, e.g. the maximum allowable junction temperature can be estimated if power, ambient temperature, and thermal resistance are known; minimum package thermal resistance can be estimated for known maximum junction temperature, ambient operating temperature, and maximum device power.

To avoid misunderstanding and misuse of the thermal equation, one should be aware that θ is not a physical property of a given package. Do not confuse θ with material thermal resistance or resistivity. The package thermal resistance, θ is an artificially derived value under a specified set of thermal testing conditions as defined by EIA/JEDEC standard. One should be cautious about drawing a correlation between the JEDEC test condition and the actual operation environment. Please refer to the JEDEC thermal test standard JESD 51 series for details.

Note: *To obtain the theoretical package thermal resistance or resistivity experimentally, the package under test should be totally insulated except for the heat flow path where the thermal resistance is being measured. In addition, only the portion of the power that flows through the heat flow path of interest should be taken into consideration, not the total power dissipated from the device.*

Similarly, T_a refers to the temperature immediately surrounding the device of interest, not necessarily the overall system ambient temperature where the device is being operated.

8.4 AMBIENT TEMPERATURE

System designers require device thermal data (θ_{ja} or θ_{jc}, or both) provided by IC makers to complete their validation of system thermal design. It is common to underestimate the actual or local ambient temperature for a device. The following guidelines on package ambient temperature, T_a, are offered to system designers to aid their understanding and more accurate use of Exar thermal data.

- Use a fine-gauge thermocouple.
- Avoid heat plume (usually a reversed cone or funnel shape) emanating from the top of package center.
- Position the thermocouple approximately 45 degrees from package edge and above the package surface around 2x package length (either X or Y whichever is longer). Refer to fig. 8 below.
- If there is a heat source or heat-generating device mounted in close proximity, position the thermocouple at the midpoint between the device of interest and the heat source.
- Case temperature measurement: When measuring package case temperature using a thermocouple, be sure that the thermocouple is properly attached to the package surface with minimal thermal resistance. Also, the heat sink effect of thermocouple may affect the temperature measurement accuracy.

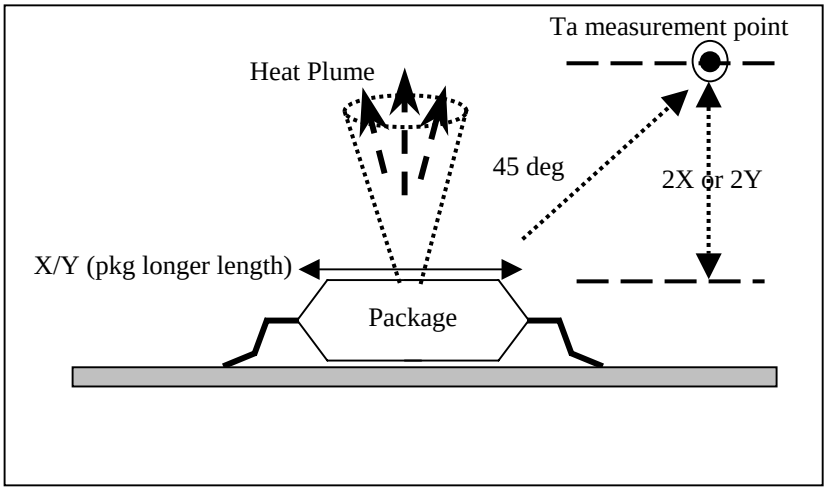


Fig. 8, Measurement of ambient temperature

8.5 OTHER VARIABLES THAT AFFECT THERMAL RESISTANCE

One also needs to consider secondary variables when making extrapolations because those variables may drastically affect package thermal resistance, for example, air flow around the device in operation, PCB substrate material, die size, die attach pad size, package internal configuration, etc. Air flow enhances heat dissipation from the device into ambient; multi-layer PCB provides better heat sink effect and helps to remove heat from devices more efficiently; larger die or die attach pad can also improve heat dissipation; external heat sink may be required when the aforementioned heat enhancements are determined to be insufficient. Please consult with Exar for your special PCB material and configuration, subsystem or system environment, or other special conditions that may invalidate the use of Exar standard thermal information.

8.6 THERMAL RESISTANCE DATA

PKG	CONFIGURATION	THETA ja C/W	THETA jc C/W	PKG	CONFIGURATION	THETA ja C/W	THETA jc C/W
PDIP	8 ld	117	56	QFP	44 ld (10x10mm)	65	18
	14 ld	90	40		52 ld (10x10mm)	61	17
	16 ld	83	35		64 ld (10x10mm)	58	16
	18 ld	75	31		44 ld (14x14mm)	56	14
	20 ld	70	28		64 ld (14x14mm)	54	13
	22 ld	67	27		80 ld (14x14mm)	48	13
	24 ld	59	25		100 ld (14x20mm)	45	12
	28 ld	57	23		120 ld (28x28mm)	38	11
	40 ld	50	22		128 ld (28x28mm)	37	11
PLCC	20 ld	49	28		144 ld (28x28mm)	36	10
	28 ld	41	21		160 ld (28x28mm)	34	9
	32 ld	40	19		208 ld (28x28mm)	32	8
	44 ld	38	16	LQFP	32 ld (7x7)	62	19
	52 ld	35	14	(1.4mmt)	48 ld (7x7)	60	17
	68 ld	29	13		44 ld (10x10)	57	15
	84 ld	26	11		64 ld (10x10)	50	11
SOIC/SOJ	8 ld	113	37		80l d (14x14)	48	9
(Jedec)	14 ld	75	32		100 ld (14x14)	46	8
	16N ld	71	27		120 ld (14x14)	44	7
	16 ld	68	25		120 ld (14x20)	43	6
	18 ld	56	23		128 ld (14x14)	44	7
	20 ld	53	22		128 ld (14x20)	43	6
	24 ld	50	21		144 ld (20x20)	42	6
	28 ld	46	20		208 ld (28x28)	40	5
SOP (5.4mm)	24 ld	60	25	TQFP	48 ld (7x7)	59	16
SSOP(5.3mm)	20 ld	81	24	(1.0mmt)	100 ld (14x14)	45	7
	24 ld	71	23	LQFP-TEP	120 ld (14x20)	21	7
	28 ld	68	21		128 ld (14x20)	20	7
TSSOP	20 ld	90	17		144ld (20x20)	18	7
(4.4mm)	28 ld	76	14		176 ld (24x24)	17	7
	38 ld	65	10		208 ld (28x28)	16	7
(6.1mm)	48 ld	58	8	PBGA	217 ball (23x23)	19	8
QSOP(.150")	28 ld	70	27		225 ball (19x19)	24	10
CDIP	14 ld	106	25		272 ball (27x27)	19	7
	18 ld	98	20		289 ball (15x15)	25	9
QFN	16 pd (4x4mm)	40	26		304 ball (31x31)	19	8
	24 pd (4x4mm)	38	26		352 ball (35x35)	17	6
	28 pd (4x4mm)	33	22		388 ball (27x27)	18	7
	32 pd (5x5mm)	33	22		388 ball (35x35)	15	6
	40 pd (6x6mm)	32	16		456 ball (27x27)	14	4
	64 pd (9x9mm)	30	10		516 ball (35x35)	16	5
					(TEP)516 ball (35x35)	13	4
TBGA	304 ball (31x31)	13	0.5		(TEP)568 ball (31x31)	12	3
	420 ball (35x35)	11.5	0.5		780 ball (37.5x37.5)	12	3
	504 ball (35x35)	11	0.5		(TEP)780 ball(37.5x37.5)	10	2
EBGA	584 ball (37.5x37.5)	10	0.5	STBGA	196 ball (12x12)	44	12
FCBGA	1397 ball (40x40)	9	0.2		196 ball (15x15)	28	10
					208 ball (17x17)	27	9

Notes: 1) The above data represent a nominal average for each package. Typical error of margin is +/-15%.
2) If the PCB is of high-conductivity type (4 layers or above), take 25% reduction from the theta ja values and 10% from theta jc values.
3) Data for PBGA is for 4-layer (4L) substrate. The above theta ja values should be increased by 15% for 2 layer substrates.
4) TEP (Thermal Enhanced Package): take 25% reduction on theta ja for exposed heat slug (TEP-1) and 15% reduction for embedded drop-in heat spreader (TEP-2).

9.0 COMMON MATERIAL CHARACTERISTICS

9.1 MOLD COMPOUND

- Used in all plastic packages, mainly for encapsulating die (IC silicon chip).
- Composition: a composite material with a mixture of silica (silicon oxide) and epoxy resin (10-20% by weight).
- Flammability (UL): UL 94-V0 rating for all mold compounds.
- Oxygen index (ASTM): 28 minimum for all mold compounds.
- Fungus-resistant for all mold compounds.
- Pb (lead) free.

9.2 SOLDER PLATING AND BALL – OUTER TREATMENT

9.2.1 ***Solder Plating:***

- Standard solder lead finish contains Sn and Pb (typical 10-20% by weight).
- Pure-Sn has been qualified by Exar and is available for most of the leaded packages upon request. Pure-Sn has been used in the IC industry for many years and has a proven track record. The concern over Sn whiskering has been shown to be invalid as long as the plating process condition is under control. In addition, pure-Sn is proven to be compatible with Pb-free and existing Sn-Pb solder pastes. Please consult with Exar's sales representative for your requirements.

9.2.2 ***Solder Ball:***

- Standard BGA solder ball contains Sn, Pb, and Ag (typical 62/32/2).
- Pb-free solder ball contains Sn/3Ag/0.5Cu.

9.3 LEAD FRAME – INNER TREATMENT

- Plastic packages use copper lead frames with minute amounts of alloy elements as mechanical-property modifiers. Inner leads and die attach pad are Ag spot plated.
- Ceramic packages use Alloy 42, Fe-Ni alloy. Inner leads are Al spot clad or deposited.

9.4 WIRES

- Plastic packages use pure gold wires for interconnection between die and leadframe or BGA substrate.
- Ceramic packages (e.g. CDIP's) use aluminum with 1-2% Si wires for interconnection between die and package.

9.5 SHIPPER MATERIAL CHARACTERISTICS

Shipper	Dimension	Material	Temperature Rating
Tube (DIP, PLCC, SOIC, SOJ, SSOP, TSSOP)	20" nom +/-0.5"	Anti-static coated PVC	Non-bakeable (40C max)
Tube (EIAJ 4.4mm SOP)	280mm nom +/-3	Anti-static coated PVC	Non-bakeable (40C max)
Tube (EIAJ 5.4mm SOP)	400mm nom +/-3	Anti-static coated PVC	Non-bakeable (40C max)
Tube (EIAJ 7.8/8.4mm SOP)	495mm nom +/-3	Conductive carbon-filled PVC	Non-bakeable (40C max)
Tube (32ld SDIP)	460mm nom +/-3	Anti-static coated PVC	Non-bakeable (40C max)
Tray (QFP, LQFP, TQFP)	135.9x315.0x7.62t mm nom +/-0.25	Static-dissipative polymer	Bakeable (135C max)
Carrier Tape	By package	Conductive polystyrene	Non-bakeable (40C max)
Cover Tape	By package	Anti-static polystyrene	Non-bakeable (40C max)
Reel	13" diameter	Anti-static coated polystyrene	Non-bakeable (40C max)
Inner Box - medium	4"x4"x22" nom +/-0.5"	Corrugated cardboard	Non-bakeable
Inner Box - small	2"x4"x22" nom +/-0.5"	Corrugated cardboard	Non-bakeable

10.0 OPERATING TEMPERATURE CLASSIFCATION

10.1 PRODUCT GRADE

Exar offers two different grades of products, commercial and industrial. The main difference is in the maximum specified operating temperature.

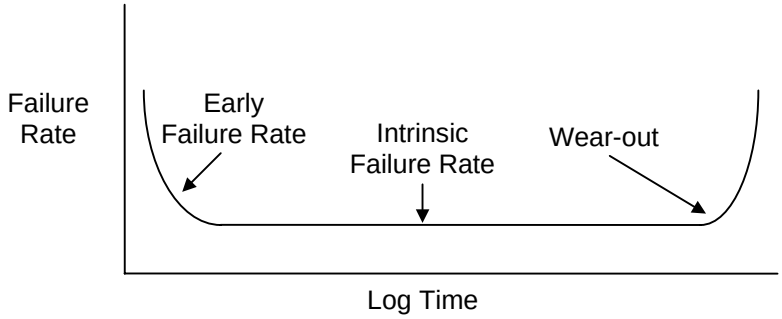
- *Commercial Grade:* operating temperature range is from 0°C to 70°C.
- *Industrial Grade:* operating temperature range is from - 40°C to 85°C.

Although product qualification tests do not make an obvious distinction between the two grades, evaluation of thermal performance does take into account the difference in operating temperature.

11.0 RELIABILITY

11.1 RELIABILITY FAILURE CURVE

Semiconductor reliability is defined in terms of a statistical probability that the device, which initially met its specification, continues to perform to specifications for a given time under stated usage conditions.



Bathtub-Shaped Failure Rate Curve

The failure rate for a particular device is not uniform throughout its life of operation. Field failures occur in distinct modes that are described by the well known "bathtub curve". The life cycle of a device is comprised of three distinct periods:

- *Early Failure Rate Period*

  Failures during this period can be attributed to latent defects from the manufacturing process. The failure rate will vary depending on the complexity, the size and the technology.

- *Intrinsic Failure Rate Period*

  This period extends for at least the next 20-30 years, during which the cumulative PPM failure may be expected to be less than 500. The failures are likely to be due to extreme or unpredictable variations in operating conditions.

- *Wear-out period*

  The onset of the wear-out period is characterized by the appearance of defects due to physical changes affecting the entire population such as wire bond thermal fatigue, irreversible chemical or metallurgical processes, and electromigration.

11.2 FAILURE RATE CALCULATIONS

The most common measure of reliability for semiconductors is the failure rate and is expressed in FITs. A FIT (Failure In Time) is one failure in 10^9 device-hours.

Failure rate estimates are based on the relationship between the failure rate of the device under working conditions and its failure rate during high temperature life-test:

$$\lambda 1 = \frac{\lambda 2}{A}$$

where:

$\lambda 1$ = failure rate at operating junction temperature
$\lambda 2$ = failure rate at life test junction temperature
A = acceleration factor.

11.3 ACCELERATION FACTOR

The acceleration factor is obtained from the Arrhenius equation:

$$A = \exp\left[\frac{-Ea}{k}\left(\frac{1}{Tj2} - \frac{1}{Tj1}\right)\right]$$

where:

A = Acceleration factor

Ea = Thermal activation energy (electron volts)
k = Boltzmann's constant (8.62 x 10E-5 eV/ °K)
Tj1 = in-use junction temperature (°K)
Tj2 = in-stress junction temperature (°K)

In order to compute the acceleration factor, the thermal activation energy of the failure mechanism and the junction temperature must be determined. Also, an adjustment for the appropriate confidence level must be made.

11.4 THERMAL ACTIVATION ENERGY

Table 1. gives the activation energy of some common types of failure mechanisms taken from published literature.

Failure Mechanism	Typical Activation Energy (eV)
Silicon Defect	0.3
Diffusion Defects	0.9
Oxide Defects	0.3
Dielectric Breakdown	0.3
Electromigraion	0.5
Ionic Contamination	1.0
Bond-Metallic Interface	1.0
Metal Corrosion	0.7

Table 1.

11.5 JUNCTION TEMPERATURE

A knowledge of junction temperature is required in order to compute the Acceleration factor. The relationship between junction temperature, ambient temperature, power dissipation and thermal resistance is given by the equation:

$$Tj = Ta + (Pd \times \theta ja)$$

where:

Tj = junction temperature (°C)
Ta = ambient temperature (°C)
Pd = power dissipation (watts)
θja = thermal resistance (°C/watt)

The power dissipation (Pd) is computed using the actual supply currents and voltages used in the life test load conditions.

The thermal resistance (θja) is a function of the packaging of the device. It is also dependent on user-controlled factors such as the method of mounting the package in its application, the proximity to heat sources or sinks and the presence or absence of air flow.

Observation (Number of Failures)	60 Percent Confidence
0	0.92
1	2.02
2	3.11
3	4.17
4	5.14
5	6.29

Table 2.

11.6 CONFIDENCE LEVEL

When a sample is selected from a population, there is always the possibility that the sample is not representative of the population at large. In particular, it is important to consider that the selected sample may have a lower failure rate than the remainder of the population.

In order to account for sampling error in the reliability computations, statistical confidence intervals are applied to the observed failure rate.

The confidence intervals are derived from Chi-square statistics. Only the upper bound of the intervals is of interest to us. Table 2. gives the upper bound of the observations at 60 percent confidence level.

For example, if the observation is 3 failures, the upper bound for the reliability computations is 4.17 at the 60 percent confidence level.

11.7 COMPUTATION EXAMPLE

A randomly selected sample of 1000 parts was subjected to a 1000-hour static life test at 125°C. The device power dissipation is 100 milliwatts and the package has a thermal resistance of 75°C/watt. The device is intended to operate in a 55°C environment.

The life test results were:

0 failure out of 1000 at 168 hours
1 failure out of 1000 at 500 hours
1 failure out of 999 at 1000 hours

The failure mode (determined by failure analysis) corresponds to an activation energy of 0.55 eV.

Total number of failures = 2
Assuming a 60 percent confidence level, the adjusted number of failures per Table 2 = 3.11

Total number of device-hours =

0(168) + (500) + 999(1000) = 999,500

Temperature rise due to power dissipation and thermal resistance:

Trise = Pd x θja = 0.1 watt x 75°C/watt = 7.5°C

Junction temperature under life test conditions:

Tj2 = 125°C + 7.5°C = 132.5°C = 405.5°K
(Note: degrees Kelvin = degrees Celsius + 273)

Failure rate under life test conditions:

λ2 = 3.11 failures / 999,500 device-hours
= 3,112 FITs at 132.5°C

Junction temperature under working conditions:

Tj1 = 55°C + 7.5°C = 62.5°C = 335.5 °K

Acceleration factor:

A = exp [- Ea/k (1/Tj2 - 1/Tj1)]

$$A = \exp\left[\frac{-0.55}{8.62 \times 10^{-5}}\left(\frac{1}{405.5} - \frac{1}{335.5}\right)\right]$$

A = 26.66

Failure rate under working environment conditions:

$$\lambda 1 = \frac{\lambda 2}{A} = \frac{3112}{26.66} = \boxed{116.7 \text{ FITS at } 55°C \text{ ambient}}$$

Also, once the failure rate is known, the MTBF (Mean Time Between Failures) can be calculated as:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

$$MTBF = \frac{1000{,}000{,}000}{116.7} = 8.569 \times 10^{6} \text{ Hours}$$

11.8 OPERATING LIFE TEST (OPL)

1. Description

This test is performed to estimate the actual Reliability performance of the product in the field. Operation of the IC under Bias at elevated temperature (i.e. 125°C) accelerates most failure mechanisms.

2. Test Condition (JESD22-A108)

- Temperature: 125°C (or 150°C)
- Read-out points: 0, 168, 500, 1000 hours (or 0, 72, 312 hours)

11.9 TEMPERATURE CYCLING TEST (T/C)

1. Description

The temperature cycle test accelerates mechanical stresses caused by thermal expansion and contraction. This mechanical stress during temperature cycling results in permanent changes in electrical characteristics, physical damage and cracking of packages.

2. Test Condition (JESD22-A104)

Step	Minutes	Temperature
COLD	≥10	-65°C (+0,-10)
HOT	≥10	150°C (-10,+15)

11.10 TEMPERATURE HUMIDITY BIAS TEST (85/85, HAST)

1. Description

The 85°C/85% R.H. or 130°C/85% R.H. (HAST) tests subject the device under test to severe conditions of temperature and humidity under Bias which accelerate the penetration of moisture through the encapsulating material, causing corrosion of the metallization.

2. Test Condition (JESD22-A101) or (JESD22-A110)

	85/85	HAST
• Temperature:	85°C (+/-2°)	130°C (+/-2°)
• Relative Humidity:	85% (+/-5%)	85% (+/-5%)
• Read-Out Point:	0, 500, 1000 hours	0, 100 hours

11.11 AUTOCLAVE TEST (Pressure Pot)

1. Description

The autoclave test subjects the Device Under Test to severe conditions of pressure, humidity and temperature not typical of actual operating environments. These conditions enhance moisture penetration through the external protective material layers (encapsulant) or along the encapsulant/conductor interface.

2. Test Condition (JESD22-A102)

- Temperature: 121°C
- Relative Humidity 100% (continuous saturated)
- Pressure 15 (+/-1) psig (2 atm)
- Duration: 96, 168 hours

11.12 HIGH TEMPERATURE STORAGE TEST (HTS)

1. Description

The High Temperature Storage test is used to evaluate both the package and die sensitivity to heat, ionic contamination and bond integrity.

2. Test Condition (JESD22-A103)

- Temperature: 150(+/-2)°C
- Read-Out Points 0, 500, 1000 hours

11.13 RELIABILITY QUALIFICATION REQUIREMENTS - GUIDELINES

TEST	INDUSTRY STANDARD	CONDITIONS	ACCEPT CRITERIA Fail/SS	TEST POINTS	ASSY QUAL	(1) NEW PRODUCT	(2) NEW FAB PROCESS
Operating Life (4)	JESD22-A108	1000 Hours @125°C	0/76	168 500 1000	X	X	X
Temperature Cycling (4)	JESD22-A104	1000 cycles -65/+150°C	0/45	500 1000	X	X	X
Pressure Pot (4)	JESD22-A102	168 Hours, 100%RH, 121°C, 2atm	0/45	96 168	X	X	X
High Temp Storage (4)	JESD22-A103	1000 Hours, Unbiased @ 150°C	0/45	500 1000	X		X
ESD Test (MM) (3)	JESD22-A115	0 Ohm, 200pf 200V	0/3	As required		X	X
ESD Test (HBM)	JESD22-A114	1500 Ohm, 100pf 2000V	0/3	As required		X	X
Temperature Humidity Bias Test (4) (6)	JESD22-A101/A110	1000 Hours, Biased 85°C/85%RH	0/45	500 1000	X		X
Latch-Up Test	JESD78	+/- 200mA or 2X Vcc @ 25°C	0/6	As required		X	X
Physical Dimension	Per Assembly Supplier Spec		0/5		X		
External Visual	Per Assembly Supplier Spec		0/15		X		
X-ray	Per Assembly Supplier Spec		0/15		X		
Mark Permanency	Per Assembly Supplier Spec		0/12		X		
Solderability	Per Assembly Supplier Spec	3 leads/unit	0/5		X		
Plating Thickness	Per Assembly Supplier Spec	3 leads/unit	0/5		X		
Lead Integrity	Per Assembly Supplier Spec	3 leads/unit	0/5		X		
Internal Visual	Per Assembly Supplier Spec		0/8		X		
Bond Pull	Per Assembly Supplier Spec	3 leads/unit	0/5		X		
SEM W/B	Per Assembly Supplier Spec	Additional Criteria: Microcracks at ball neck	0/2		X		
Cratering	Per Assembly Supplier Spec		0/5		X		
Ld Fin Adhesion	Per Assembly Supplier Spec	3 leads/unit	0/5		X		
Ball Shear	Per Assembly Supplier Spec	all bonds	0/5		X		
Die Shear	Per Assembly Supplier Spec		0/5		X		
Moisture Sensitivity	JEDEC-STD 020	As defined	N/A	Note 5	X		

Notes: 1) Op-Life, Temp Cycle, and Pressure Pot can be satisfied by similarity.
2) 2 wafer lots are used for qualification, ESD and Latch-up will be done on one lot only.
3) ESD (machine model) is done if requested by customer.
4) Preconditioning is done prior to stress.

5) For MSL classification only.
6) HAST conditions (100 Hours, 130°C/ 85% RH) may be used.

11.14 ONGOING RELIABILITY MONITORING

Test	Industry Standard	Conditions	Accept Criteria Fail/Ss	Test Points	Frequency	Coverage
Early Failure Rate (2)		168 Hours @ 125°C	0/45	168 Hours	Quarterly	0.6u CMOS .0.35u CMOS
Op Life (2)	JESD22-A108	1000 Hours @125°C	0/45	1000 Hours	Quarterly	0.6u CMOS 0.35u CMOS
Temperature Cycling (1)	JESD22-A104	1000 cycles -65/+150°C	0/45	1000 Cycles	Quarterly	Every package family
Pressure Pot (1)	JESD22-A102	168 Hours, 100%RH, 121°C, 2atm	0/45	168 Hours	Monthly	Every package family
High Temp Storage	JESD22-A103	1000 Hours, @ 150°C	0/45	1000 Hours	Quarterly	0.6u CMOS 0.35u CMOS
Temperature Humidity Bias Test (1) (3)	JESD22-A101/ A110	1000 Hours, Biased 85°C/85%RH	0/45	1000 Hours	Quarterly	Fab/Mold Compound

Note: 1) Surface mount packages will receive preconditioning prior to assembly related tests.
2) Early failure and Op-life tests can be done at 150°C, time points will be at 72/312 hours.
3) HAST conditions (100 Hours, 130°C/ 85% RH) may be used.